MT6592
Octa-Core Smartphone Application Processor Technical Brief

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Document Revision History

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1 System Overview

MT6592 is a highly integrated baseband platform incorporating modem, application processing and connectivity subsystems to enable 3G smart phone applications. The chip integrates a Octa-core ARM® Cortex-A7 MPCore™ operating up to 1.7GHz, an ARM® Cortex-R4 MCU and a powerful multi-standard video accelerator. The MT6592 interfaces to NAND flash memory, LPDDR2 and LPDDR3 for optimal performance and also supports booting from SLC NAND or eMMC to minimize the overall BOM cost. In addition, an extensive set of interfaces are included to interface to cameras, touch-screen displays, and MMC/SD cards.

The application processor, a Octa-core ARM® Cortex-A7 MPCore™ which includes a NEON multimedia processing engine, offers processing power necessary to support the latest OpenOS along with its demanding applications such as web browsing, email, GPS navigation and games. All are viewed on a high resolution touch screen display with graphics enhanced by the 3D graphics acceleration. The multi-standard video accelerator and an advanced audio subsystem are also included to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders such as H.264 and MPEG-4. Audio supports include FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR vocoders, polyphonic ringtones and advanced audio functions such as echo cancellation, hands-free speakerphone operation and noise cancellation.

An ARM® Cortex-R4, DSP, and 2G and 3G coprocessors provide a powerful modem subsystem capable of supporting Category 14 (21 Mbps) HSDPA downlink and Category 6 (5.76 Mbps) HSUPA uplink data rates as well as Class 12 GPRS, EDGE.

MT6592 includes four wireless connectivity functions, WLAN, Bluetooth, GPS, and FM receiver. The RF parts of those four blocks are put in the MT6625 chip. With four advanced radio technologies integrated into one single chip, MT6592/MT6625 provides the best and most convenient connectivity solution among the industry. MT6592/MT6625 implements advanced and sophisticated Radio Coexistence algorithms and hardware mechanisms. It also supports single antenna sharing among 2.4 GHz antenna for Bluetooth, WLAN and 1.575 GHz for GPS. The enhanced overall quality is achieved for simultaneous voice, data, and audio/video transmission on mobile phones and Media Tablets. The small footprint with low-power consumption greatly reduces the PCB layout resource.

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1.1 Platform Features

- **General**
  - Smartphone two MCU subsystems architecture
  - SLC NAND flash and eMMC bootloader
- **AP MCU subsystem**
  - Octa-core ARM® Cortex-A7 MPCore™ operating at 1.7 GHz
  - NEON multimedia processing engine with SIMDv2 / VFPv4 ISA support
  - 32KB L1 I-cache and 32KB L1 D-cache
  - 1MB L2 cache
  - DVFS technology with adaptive operating voltage from 0.9V to 1.15V
- **MD MCU subsystem**
  - ARM® Cortex-R4 processor with maximum 491.52 MHz operation frequency
  - 32KB I-cache, 16KB D-cache
  - 256KB TCM (tightly-coupled memory)
  - DSP for running modem/voice tasks, with maximum 240MHz operation frequency
  - High-performance AXI and AHB bus
  - General DMA engine and dedicated DMA channels for peripheral data transfer
  - Watchdog timer for system error recovery
  - Power management for clock gating control
- **CONN MCU subsystem**
  - Andes N9 processor with 32KB I-cache, 16KB D-cache
- **MD external interfaces**
  - Dual SIM/USIM interface supported
  - Interface pins with RF and radio-related peripherals (antenna tuner, PA, …)
- **External memory interface**
  - Supports LPDDR2/3 up to 2GB
  - 32-bit data bus width
  - Memory clock up to 667 MHz
  - Supports self-refresh/partial self-refresh mode
  - Low-power operation
  - Programmable slew rate for memory controller's IO pads
  - Supports dual rank memory device
  - Advanced bandwidth arbitration control
- **Security**
  - ARM® TrustZone® Security
- **Connectivity**
  - USB2.0 high-speed dual mode supporting 8 Tx and 8 Rx endpoints
  - NAND flash controller supporting NAND bootable, iNAND2® and MoviNAND®
  - 4 UARTs for external devices and debugging interfaces
  - SPI master for external devices
  - 3 I2C to control peripheral devices, e.g. CMOS image sensor, or LCM module
  - I2S master output and master/slave input for connection with optional external hi-end audio codec
  - GPIOs
  - 3 sets of memory card controller supporting

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SD/SDHC/MS/MSPRO/MMC and SDIO2.0/3.0 protocols

- **Operating conditions**
  - Core voltage: 1.0V
  - Processor DVFS+SRAM voltage : 0.9V~1.15V (Typ. 1.0V ; sleep mode 0.7V)
  - I/O voltage: 1.8V/2.8V/3.3V
  - Memory: 1.2V
  - NAND: 1.8V/2.8V
  - LCM interface: 1.8V
  - Clock source: 26-MHz, 32.768-kHz

- **Package**
  - Type: FCCSP
  - 10.6mm x 11mm
  - Height: 1.0mm maximum
  - Ball count: 475 balls
  - Ball pitch: 0.4mm

1.2 MODEM Features

- **3G UMTS FDD supported features (with MT6166)**
  - CPC (DTX in CELL_DCH, UL DRX DL DRX), HS-SCCH-less, HS-DSCH
  - MAC-ehs
  - Uplink Cat. 6, throughput up to 5.7Mbps
  - Downlink Cat. 14, throughput up to 21Mbps
  - Fast dormancy
  - ETWS
  - Network selection enhancements

- **Radio interface and baseband front-end**
  - High dynamic range delta-sigma ADC converts the downlink analog I and Q signals to digital baseband
  - 10-bit D/A converter for Automatic Power Control (APC)
  - Programmable radio Rx filter with adaptive gain control
  - Dedicated Rx filter for FB acquisition
  - Baseband Parallel Interface (BPI) with programmable driving strength (shared by 2G & 3G modem)
  - Supports multi-band

- **GSM modem and voice CODEC**
  - Dial tone generation
  - Noise reduction
  - Echo suppression
  - Advanced sidetone oscillation reduction
  - Digital sidetone generator with programmable gain
  - Two programmable acoustic compensation filters
  - GSM quad vocoders for adaptive multirate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
  - GSM channel coding, equalization and A5/1, A5/2 and A5/3 ciphering
  - GPRS GEA1, GEA2 and GEA3 ciphering
  - Programmable GSM/GPRS/EDGE modem
  - Packet switched data with CS1/CS2/CS3/CS4 coding schemes
  - GSM circuit switch data
  - GPRS/EDGE Class 12
  - Supports SAIC (single antenna interference cancellation) technology
  - Supports VAMOS (Voice services over Adaptive Multi-user channels on One Slot) technology in R9 spec

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1.3 Multimedia Features

- **Display**
  - Supports portrait panel resolution up to FHD (1920x1080)
  - MIPI DSI interface (4 data lanes)
  - Embedded LCD gamma correction
  - Supports true colors
  - 4 overlay layers with per-pixel alpha channel and gamma table
  - Supports spatial and temporal dithering
  - Supports side-by-side format output to stereo 3D panel in both portrait and landscape modes
  - Supports color enhancement
  - Supports adaptive contrast enhancement
  - Supports image/video/graphic sharpness enhancement
  - Supports dynamic backlight scaling

- **Graphics**
  - OpenGL ES 1.1/2.0 3D graphic accelerator capable of processing 152.25M tri/sec and 2800M pixel/sec @ 700MHz
  - OpenVG1.1 vector graphics accelerator

- **Image**
  - Integrated image signal processor supports 13 MP
  - Supports electronic image stabilization
  - Supports video stabilization
  - Supports preference color adjustment
  - Supports noise reduction
  - Supports lens shading correction
  - Supports auto sensor defect pixel correction
  - Supports AE/AWB/AF
  - Supports edge enhancement (sharpness)
  - Supports face detection and visual tracking
  - Supports zero shutter delay image capture
  - Supports capturing full size image when recording video (up to 13M sensor)
  - Supports MIPI CSI-2 high-speed camera serial interface with 4 data lane (for main) + 2 data lane (for sub)
  - Hardware JPEG encoder: Baseline encoding with 120M pixel/sec
  - Supports YUV422/YUV420 color format and EXIF/JFIF format

- **Video**
  - HEVC decoder 1080p @ 30fps
  - VP9 decoder 1080p @ 30fps
  - H.264 decoder: Baseline 1080p @ 30fps/40Mbps
  - H.264 decoder: Main/high profile 1080p@30fps/40Mbps
  - Sorenson H.263/H.263 decoder: 1080p @ 30fps/40Mbps
  - MPEG-4 SP/ASP decoder: 1080p @ 30fps/40Mbps
  - DIVX4/DIVX5/DIVX6/DIVX HD/XVID decoder: 1080p @ 30fps/40Mbps
  - VP8 decoder: 1080p @ 30fps/6Mbps (SW)
  - VC-1 decoder: 1080p @ 30fps/20Mbps (SW)
  - MPEG-4 encoder: Simple profile D1 @ 30fps (SW)
  - H.263 encoder: D1 @ 30fps (SW)
  - H.264 encoder: High profile 1080p @ 30fps

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- **Audio**
  - Sampling rates supported: 8kHz to 48kHz
  - Sample formats supported: 8-bit/16-bit/24-bit, Mono/Stereo
  - Interfaces supported: I2S, PCM
  - External CODEC I2S interface supports up to 24-bit sample
  - 4-band IIR compensation filter to enhance loudspeaker responses
  - Proprietary audio post-processing technologies: BesLoudness, Android built-in post processing
  - Audio encode: AMR-NB, AMR-WB, AAC, OGG, ADPCM
  - Audio decode: WAV, MP3, MP2, AAC, AMR-NB, AMR-WB, MIDI, Vorbis, APE, AAC-plus v1, AAC-plus v2, FLAC, WMA, ADPCM

- **Speech**
  - Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR)
  - CTM
  - Noise reduction
  - Noise suppression
  - Noise cancellation
  - Dual-MIC noise cancellation
  - Echo cancellation
  - Echo suppression
  - Dual-MIC input
  - Digital MIC input

1.4 BT/WLAN/GPS/FM with MT6625 Features

- **Common**
  - Self calibration
  - Single TCXO and TSX for GPS, BT and WLAN
  - Best-in-class current consumption performance
  - OS supported: Android
  - Intelligent BT/WLAN coexistence scheme
  - Single antenna support for WLAN/Bluetooth/GPS

- **WLAN**
  - Dual-band (2.4GHz and 5GHz) single stream 802.11 a/b/g/n RF
  - 802.11 d/h/k compliant
  - Security: WFA WPA/WPA2 personal, WPS2.0, WAPI (hardware)
  - QoS: WFA WMM, WMM PS
  - Supports 802.11n optional features: STBC, A-MPDU, Blk-Ack, RIFS, MCS Feedback, 20/40MHz coexistence (PCO), unscheduled PSMP
  - Supports 802.11w Protected Managed Frames
  - Supports WiFi Direct (WFA P-2-P standard) and Wi-Fi Miracast (Wi-Fi Display)
  - Supports Wi-Fi HotSpot 2.0
  - Integrated PA with max 21dBm output power
  - Typical -77.5 dBm 2.4GHz receiver sensitivity at 11g 54Mbps mode
  - Per packet TX power control

- **Bluetooth**
  - Bluetooth specification v2.1+EDR
  - Bluetooth specification 3.0+HS compliance
  - Bluetooth v4.0 Low Energy (LE)
  - Integrated PA with 10dBm (class 1) transmit power and Balun

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- Rx sensitivity: GFSK -95dBm, DQPSK -94dBm, 8-DPSK -88dBm
- Best-in-class BT/Wi-Fi coexistence performance
- Up to 4 piconets simultaneously with background inquiry/page scan
- Supports Scatternet
- Packet loss concealment (PLC) function for better voice quality
- Low-power scan function to reduce the power consumption in scan modes

- **GPS**
  - Supports GPS/QZSS/SBAS (WAAS/MSAS/EGNOS/GAGAN)
  - Best-in-class sensitivity performance
    - -165 dBm tracking sensitivity
    - -163 dBm hot start sensitivity
    - -148 dBm cold start sensitivity
    - -151 dBm warm start sensitivity
  - AGPS sensitivity is 6dB design margin over 3GPP
  - Full A-GPS capability (E911/SUPL/EPO/HotStill)
  - Active interference cancellation for up to 8 in-band tones
  - Supports TCXO
  - Supports co-clock with AP/MD
  - 5Hz update rate

- **FM**
  - 65-108MHz with 50kHz step
  - Supports RDS/RBDS
  - Digital stereo modulator/demodulator
  - Simplified digital audio interface (I2S)
  - Fast seek time 30ms/channel
  - Stereo noise reduction
  - Audio sensitivity 2dBμVemf ((S+N)/N=26dB)
  - Audio S/N 60dB
  - Anti-jamming
  - Integrated short antenna

- **WBT IPD**
  - Integrated matching network, balance band-pass filter, GPS-WBT diplexer.
  - Fully integrated in one IPD die
  - Supports single and dual antenna operation.

- **GPS IPD**
  - Integrated high-pass type matching network and 5^{th}-order ellipse low-pass filter.
  - Fully integrated in one IPD die
  - Supports single and dual antenna operation.

1.5 General Descriptions

MediaTek MT6592 is a highly integrated 3G System-on-chip (SoC) which incorporates advanced features e.g. HSPA R8 modem, Octa-core ARM® Cortex-A7 MPCore™ operating at 1.7GHz, 3D graphics (OpenGL|ES 2.0), 13M camera ISP, LPDDR2/3 667 MHz and high-definition 1080p video decoder. MT6592 helps phone manufacturers build high-performance 3G smart phones with PC-like browser, 3D gaming and cinema class home entertainment experiences.

World-leading technology

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Based on MediaTek's world-leading mobile chip SoC architecture with advanced 28nm process, MT6592 is the brand-new generation smart phone SoC integrating MediaTek HSPA R8 modem, 1.7GHz Octa-core ARM® Cortex-A7 MPCore^{TM}, 3D graphics and high-definition 1080p video decoder.

Rich in features, high-valued product

To enrich the camera features, MT6592 equips a 13M camera ISP with advanced features e.g. auto focus, anti-handshake, auto sensor defect pixel correction, continuous video AF, face detection, burst shot, optical zoom, panorama view and 3D photos.

Incredible browser experience

The 1.7GHz Octa-core ARM® Cortex-A7 MPCore^{TM} with NEON multimedia processing engine brings PC-like browser experiences and helps accelerate OpenGL|ES 2.0 3D Adobe Flash 10 rendering performance to an unbeatable level.

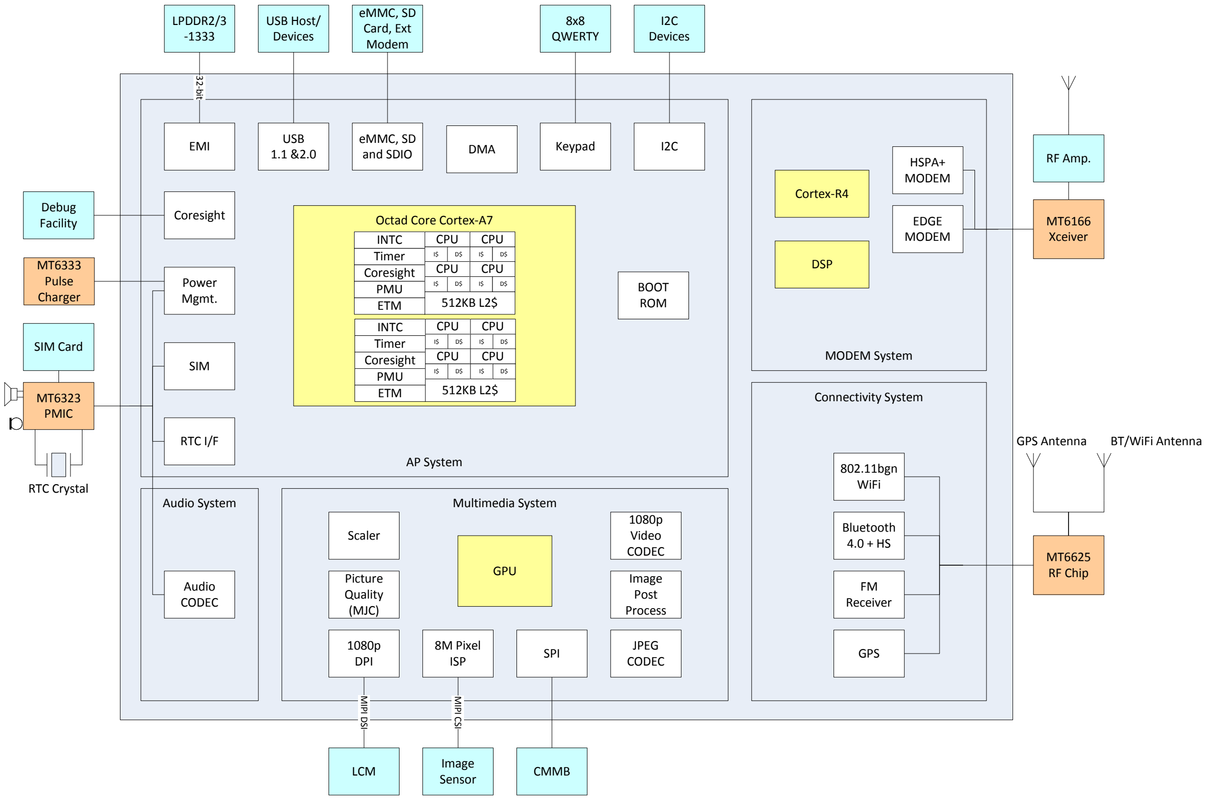

Figure 1-1. Block diagram of MT6592

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2 Product Description

2.1 Pin Description

2.1.1 Ball Map View

475	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	TP_MEMPLL	AVSS18_MEM	AVDD18_ME	RA9	RA6		RA4	RA3		RDQ19	RDQ23		RDQ21	RDQ22		RDQ4	RDQ6		DVSS	RDQ9		RDQ12	RDQ25		RDQ29	DVSS	A
B	CMPCLK	CMMCLK	REXTDN	DVSS	RCKE	RCS1_B	RCS0_B	RA0	RA1	DVSS	RDQ16	DVSS	RDQ18	DVSS	RDQ3	RDQ7	DVSS	RDQ5	RDQ10	RDQ14	RDQ8	DVSS	RDQ26	DVSS	RDQ28	RDQ27	B
C		MSDC1_DAT2	MSDC1_CLK	DVSS		RA8	RA5	DVSS		RDQ17	DVSS	DVSS		RDQ0	RDQ2	DVSS	DVSS	DVSS	RDQ11	DVSS	DVSS	DVSS	DVSS	RDQ30	DVSS	RDQ31	C
D	DVDD18_IO2	MSDC1_DAT1	MSDC1_DAT3	DVSS	DVSS	RA7	DVSS	RA2	DVSS	RDQM2	DVSS	RDQ20	DVSS	RDQ1	DVSS	RDQM0	DVSS	RDQM1		RDQ13	DVSS	RDQ15	RDQM3	DVSS	RDQ24	MSDC0_CLK	D
E	DVDD28_MSD	CMDAT0	MSDC1_CMD	MSDC1_DAT0	DVSS		DVDD12_EMI	DVSS	RCLK0	DVSS		RDQS2_B			RDQS0_B		RDQS1_B	DVSS		RDQS3	DVSS		MSDC0_DAT6	MSDC0_CMD	MSDC0_DAT2	MSDC0_DAT3	E
F		CMDAT1			RCP_A	DVSS	DVDD12_EMI	DVDD12_EMI	RCLK0_B			RDQS2			RDQS0	VREF	RDQS1	DVSS		RDQS3_B		MSDC0_DAT7		MSDC0_DAT5			F
G	DVDD18_MIPII	RDP3	RDN0_A	RDP0_A	RCN_A	DVSS	DVSS	DVDD12_EMI	DVDD12_EMI		DVDD12_EMI		DVDD12_EMI	DVSS	DVDD12_EMI	DVDD12_EMI	DVSS	DVDD12_EMI		DVSS		MSDC0_DAT0	MSDC0_DAT1	MSDC0_DAT4	MSDC0_RSTB	DVDD18_MSD	G
H		RDN3	RDN1_A	DVSS18_MIPII	DVSS18_MIPII			DVDD12_EMI		DVSS	DVDD12_EMI	DVSS	DVDD12_EMI	DVSS	DVDD12_EMI	DVDD12_EMI	DVSS	DVDD12_EMI		DVSS		PWRAP_SPI0_	PWRAP_SPI0_	PWRAP_INT			H
J	RDP2	RDN2	RDP1_A		DVSS18_MIPII		DVSS18_MIPII														DVSS		PWRAP_SPI0_	PWRAP_SPI0_	AUD_DAT_MO		J
K	RDP1	RDN1	RDN0		RCN	RCP															DVSS		SIM1_SIO	SIM2_SRST	AUD_DAT_MIS	AUD_CLK_MO	K
L		DVDD18_MIPI	RDP0	DVSS18_MIPIT						DVSS	VCCK	VCCK	VCCK	VCCK	VCCK	VCCK	VCCK	DVSS		SIM2_SCLK	SIM1_SCLK		SIM1_SRST	SIM2_SIO	RTC32K_CK	DVDD18_IO0	L
M	TDP0	TDN0	TCP	TCN	TDN3		DVSS18_MIPIT	DVSS18_MIPIT		VCCK	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	VCCK		DVSS				SRCLKENAI	SYSRSTB		M
N	VRT	TDN1	DVSS18_MIPIT		TDP3					VCCK	DVSS	VCCK_VPROC	VCCK_VPROC	VCCK_VPROC	VCCK_VPROC	VCCK_VPROC	VCCK_VPROC	VCCK			DVSS		CHD_DP	CHD_DM	SRCLKENA	WATCHDOG	N
P	TDP2	TDP1							VCCK	DVSS	DVSS	DVSS	DVSS	VCCK_VPROC	VCCK_VPROC	DVSS	DVSS	VCCK			DVSS	URXD2	UTXD2		USB_VRT	AVDD18_USB	P
R	TDN2	DVSS		DVDD18_EFUS	FSOURCE_P		MSDC2_CLK		VCCK	VCCK	DVSS	VCCK_VPROC	VCCK_VPROC	VCCK_VPROC	VCCK_VPROC	VCCK_VPROC	VCCK_VPROC	VCCK					URXD3	AVSS33_USB	USB_DM	USB_DP	R
T	MSDC2_DAT2	MSDC2_DAT3	MSDC2_CMD		MSDC2_DAT1	MSDC2_DAT0				VCCK	DVSS	DVSS	DVSS	VCCK_VPROC	VCCK_VPROC	DVSS	DVSS	DVSS			DVSS		UTXD3	AVDD33_USB			T
U		UTXD1	LCM_RST		I2S_LRCK		AVSS18_WBG			VCCK	DVSS	DVSS			VCCK_VPROC	VCCK_VPROC	AVSS18_AP	AVSS18_AP		AVSS18_MD	AVSS18_MD			PCM_TX	DVDD18_IO1		U
V	DVDD28_MSD	URXD1			I2S_BCK		AVSS18_WBG			VCCK	DVSS	DVSS	DVSS	DVSS	VCCK_VPROC	VCCK_VPROC	AVSS18_AP	AVSS18_AP		AVSS18_MD	AVSS18_MD	EINT1	PCM_CLK	EINT3	PCM_SYNC	PCM_RX	V
W	DVDD18_IO3	URXD0			I2S_DATA_IN		AVSS18_WBG													AVSS18_MD	AVSS18_MD	EINT0			EINT4		W
Y		UTXD0	DSI_TE			WB_CRTL0	AVSS18_WBG			F2W_DATA			KPCOL2	BSI_CLK	BPI_BUS15					AVSS18_MD	AVSS18_MD	EINT10	EINT9		EINT5	DVDD18_IO1	Y
AA	SCL2	SDA2	SCL0	WB_CRTL3	WB_CRTL2	WB_CRTL1				F2W_CLK			KPROW2	BSI_DATA1			BPI_BUS8	AVSS18_AP			AVSS18_MD		EINT6	EINT2	EINT8	EINT7	AA
AB			SDA0	WB_CRTL5	WB_CRTL4	AVSS18_WBG		AVSS18_WBG	SPI_MI				KPCOL0	BSI_DATA0			BPI_BUS13		AVSS18_AP		AVSS18_MD		BPI_BUS1	BPI_BUS0	ANT_SEL0		AB
AC	WB_RXIP	WB_RXIN	AVSS18_WBG		AVSS18_WBG		AVSS18_WBG	SPI_CS	SPI_MO	EINT20	EINT17		KPROW0	BSI_DATA2	BPI_BUS14	BPI_BUS10	BPI_BUS12		AUX_IN0		AVSS18_MD		BPI_BUS4	BPI_BUS3	ANT_SEL2	ANT_SEL1	AC
AD		WB_RXQP		AVSS18_WBG		XIN_WBG	SPI_CK	SCL1	DISP_PWM	EINT18			KPCOL1	BSI_EN		BPI_BUS9			AUX_IN1			AVSS18_MD		BPI_BUS6	BPI_BUS2	DVDD28_BPI	AD
AE	WB_TXIP	WB_RXQN	AVSS18_WBG	AVDD18_WBG	AVSS18_WBG	WB_SEN	SDA1		EINT19	EINT16		JTDO	KPROW1	TXBPI				DVDD18_PLLG	AVDD18_AP		AVDD18_MD	AVDD28_DAC		APC	BPI_BUS5		AE
AF	WB_TXIN	WB_TXQN	AVSS18_WBG	GPS_RXIP	GPS_RXQN	WB_RSTB	WB_SDATA	EINT14	GPIO13	EINT11	TESTMODE	JTCK	JTMS	VM1	BPI_BUS11	BPI_BUS7	AUX_YP	AUX_XP	AVSS_REFN	UL_Q_N	UL_I_N	UL_I_P			VBIAS	CLK26M	AF
AG	AVSS18_WBG	WB_TXQP		GPS_RXIN	GPS_RXQP		WB_SCLK	EINT15		GPIO12	JTDI		DVDD18_IO4	VM0		AUX_YM	AUX_XM		REFP	UL_Q_P		DL_Q_P	DL_Q_N	DL_I_N	DL_I_P	AVSS18_MD	AG
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 2-1. LPDDR2 ball map view of MT6592

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475	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	TP_MEMPLL	AVSS18_MEM	AVDD18_ME	RA9	RA6		RA4	RA3		RDQ17	RDQ20		RDQ23	RDQ22		RDQ6	RDQ5		DVSS	RDQ9		RDQ15	RDQ25		RDQ31	DVSS	A
B	CMPCLK	CMMCLK	REXTDN	DVSS	RCKE	RCS1_B	RCS0_B	RA0	RA1	DVSS	RDQ16	DVSS	RDQ19	DVSS	RDQ2	RDQ4	DVSS	RDQ7	RDQ8	RDQ11	RDQ14	DVSS	RDQ27	DVSS	RDQ28	RDQ30	B
C		MSDC1_DAT2	MSDC1_CLK	DVSS		RA8	RA5	DVSS		RDQ18	DVSS	DVSS		RDQ0	RDQ3	DVSS	DVSS	DVSS	RDQ10	DVSS	DVSS	DVSS	DVSS	RDQ24	DVSS	RDQ29	C
D	DVDD18_IO2	MSDC1_DAT1	MSDC1_DAT3	DVSS	DVSS	RA7	DVSS	RA2	DVSS	RDQM2	DVSS	RDQ21	DVSS	RDQ1	DVSS	RDQM0	DVSS	RDQM1		RDQ12	DVSS	RDQ13	RDQM3	DVSS	RDQ26	MSDC0_CLK	D
E	DVDD28_MSD	CMDAT0	MSDC1_CMD	MSDC1_DAT0	DVSS		DVDD12_EMI	DVSS	RCLK0	DVSS		RDQS2_B			RDQS0_B		RDQS1_B	DVSS		RDQS3	DVSS		MSDC0_DAT6	MSDC0_CMD	MSDC0_DAT2	MSDC0_DAT3	E
F		CMDAT1			RCP_A	DVSS	DVDD12_EMI	DVDD12_EMI	RCLK0_B			RDQS2			RDQS0	VREF	RDQS1	DVSS		RDQS3_B		MSDC0_DAT7		MSDC0_DAT5			F
G	DVDD18_MIPII	RDP3	RDN0_A	RDP0_A	RCN_A	DVSS	DVSS	DVDD12_EMI	DVDD12_EMI		DVDD12_EMI		DVDD12_EMI	DVSS	DVDD12_EMI	DVDD12_EMI	DVSS	DVDD12_EMI		DVSS		MSDC0_DAT0	MSDC0_DAT1	MSDC0_DAT4	MSDC0_RSTB	DVDD18_MSD	G
H		RDN3	RDN1_A	DVSS18_MIPII	DVSS18_MIPII			DVDD12_EMI		DVSS	DVDD12_EMI	DVSS	DVDD12_EMI	DVSS	DVDD12_EMI	DVDD12_EMI	DVSS	DVDD12_EMI		DVSS		PWRAP_SPI0_	PWRAP_SPI0_	PWRAP_INT			H
J	RDP2	RDN2	RDP1_A		DVSS18_MIPII		DVSS18_MIPII														DVSS		PWRAP_SPI0_	PWRAP_SPI0_	AUD_DAT_MO		J
K	RDP1	RDN1	RDN0		RCN	RCP															DVSS		SIM1_SIO	SIM2_SRST	AUD_DAT_MIS	AUD_CLK_MO	K
L		DVDD18_MIPI	RDP0	DVSS18_MIPIT						DVSS	VCCK	VCCK	VCCK	VCCK	VCCK	VCCK	VCCK	DVSS		SIM2_SCLK	SIM1_SCLK		SIM1_SRST	SIM2_SIO	RTC32K_CK	DVDD18_IO0	L
M	TDP0	TDN0	TCP	TCN	TDN3		DVSS18_MIPIT	DVSS18_MIPIT		VCCK	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	VCCK		DVSS				SRCLKENAI	SYSRSTB		M
N	VRT	TDN1	DVSS18_MIPIT		TDP3					VCCK	DVSS	VCCK_VPROC	VCCK_VPROC	VCCK_VPROC	VCCK_VPROC	VCCK_VPROC	VCCK_VPROC	VCCK			DVSS		CHD_DP	CHD_DM	SRCLKENA	WATCHDOG	N
P	TDP2	TDP1							VCCK	DVSS	DVSS	DVSS	DVSS	VCCK_VPROC	VCCK_VPROC	DVSS	DVSS	VCCK			DVSS	URXD2	UTXD2		USB_VRT	AVDD18_USB	P
R	TDN2	DVSS		DVDD18_EFUS	FSOURCE_P		MSDC2_CLK		VCCK	VCCK	DVSS	VCCK_VPROC	VCCK_VPROC	VCCK_VPROC	VCCK_VPROC	VCCK_VPROC	VCCK_VPROC	VCCK					URXD3	AVSS33_USB	USB_DM	USB_DP	R
T	MSDC2_DAT2	MSDC2_DAT3	MSDC2_CMD		MSDC2_DAT1	MSDC2_DAT0				VCCK	DVSS	DVSS	DVSS	VCCK_VPROC	VCCK_VPROC	DVSS	DVSS	DVSS			DVSS		UTXD3	AVDD33_USB			T
U		UTXD1	LCM_RST		I2S_LRCK		AVSS18_WBG			VCCK	DVSS	DVSS			VCCK_VPROC	VCCK_VPROC	AVSS18_AP	AVSS18_AP		AVSS18_MD	AVSS18_MD			PCM_TX	DVDD18_IO1		U
V	DVDD28_MSD	URXD1			I2S_BCK		AVSS18_WBG			VCCK	DVSS	DVSS	DVSS	DVSS	VCCK_VPROC	VCCK_VPROC	AVSS18_AP	AVSS18_AP		AVSS18_MD	AVSS18_MD	EINT1	PCM_CLK	EINT3	PCM_SYNC	PCM_RX	V
W	DVDD18_IO3	URXD0			I2S_DATA_IN		AVSS18_WBG													AVSS18_MD	AVSS18_MD	EINT0			EINT4		W
Y		UTXD0	DSI_TE			WB_CRTL0	AVSS18_WBG			F2W_DATA			KPCOL2	BSI_CLK	BPI_BUS15					AVSS18_MD	AVSS18_MD	EINT10	EINT9		EINT5	DVDD18_IO1	Y
AA	SCL2	SDA2	SCL0	WB_CRTL3	WB_CRTL2	WB_CRTL1				F2W_CLK			KPROW2	BSI_DATA1			BPI_BUS8	AVSS18_AP			AVSS18_MD		EINT6	EINT2	EINT8	EINT7	AA
AB			SDA0	WB_CRTL5	WB_CRTL4	AVSS18_WBG		AVSS18_WBG	SPI_MI				KPCOL0	BSI_DATA0			BPI_BUS13		AVSS18_AP		AVSS18_MD		BPI_BUS1	BPI_BUS0	ANT_SEL0		AB
AC	WB_RXIP	WB_RXIN	AVSS18_WBG		AVSS18_WBG		AVSS18_WBG	SPI_CS	SPI_MO	EINT20	EINT17		KPROW0	BSI_DATA2	BPI_BUS14	BPI_BUS10	BPI_BUS12		AUX_IN0		AVSS18_MD		BPI_BUS4	BPI_BUS3	ANT_SEL2	ANT_SEL1	AC
AD		WB_RXQP		AVSS18_WBG		XIN_WBG	SPI_CK	SCL1	DISP_PWM	EINT18			KPCOL1	BSI_EN		BPI_BUS9			AUX_IN1			AVSS18_MD		BPI_BUS6	BPI_BUS2	DVDD28_BPI	AD
AE	WB_TXIP	WB_RXQN	AVSS18_WBG	AVDD18_WBG	AVSS18_WBG	WB_SEN	SDA1		EINT19	EINT16		JTDO	KPROW1	TXBPI				DVDD18_PLLG	AVDD18_AP		AVDD18_MD	AVDD28_DAC		APC	BPI_BUS5		AE
AF	WB_TXIN	WB_TXQN	AVSS18_WBG	GPS_RXIP	GPS_RXQN	WB_RSTB	WB_SDATA	EINT14	GPIO13	EINT11	TESTMODE	JTCK	JTMS	VM1	BPI_BUS11	BPI_BUS7	AUX_YP	AUX_XP	AVSS_REFN	UL_Q_N	UL_I_N	UL_I_P			VBIAS	CLK26M	AF
AG	AVSS18_WBG	WB_TXQP		GPS_RXIN	GPS_RXQP		WB_SCLK	EINT15		GPIO12	JTDI		DVDD18_IO4	VM0		AUX_YM	AUX_XM		REFP	UL_Q_P		DL_Q_P	DL_Q_N	DL_I_N	DL_I_P	AVSS18_MD	AG
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 2-2. LPDDR3 ball map view of MT6592

2.1.1 Pin Coordinate

Table 2-1. LPDDR2 pin coordinate

Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
A1	TP_MEMPLL	H18	DVDD12_EMI	V20	AVSS18_MD
A2	AVSS18_MEMPLL	H20	DVSS	V21	AVSS18_MD
A3	AVDD18_MEMPLL	H22	PWRAP_SPI0_MO	V22	EINT1
A4	RA9	H23	PWRAP_SPI0_CK	V23	PCM_CLK

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Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
A5	RA6	H24	PWRAP_INT	V24	EINT3
A7	RA4	J1	RDP2	V25	PCM_SYNC
A8	RA3	J2	RDN2	V26	PCM_RX
A10	RDQ19	J3	RDP1_A	W1	DVDD18_IO3
A11	RDQ23	J5	DVSS18_MIPIIO	W2	URXD0
A13	RDQ21	J7	DVSS18_MIPIIO	W5	I2S_DATA_IN
A14	RDQ22	J21	DVSS	W7	AVSS18_WBG
A16	RDQ4	J23	PWRAP_SPI0_CSN	W20	AVSS18_MD
A17	RDQ6	J24	PWRAP_SPI0_MI	W21	AVSS18_MD
A19	DVSS	J25	AUD_DAT_MOSI	W22	EINT0
A20	RDQ9	K1	RDP1	W25	EINT4
A22	RDQ12	K2	RDN1	Y2	UTXD0
A23	RDQ25	K3	RDN0	Y3	DSI_TE
A25	RDQ29	K5	RCN	Y6	WB_CRTL0
A26	DVSS	K6	RCP	Y7	AVSS18_WBG
B1	CMPCLK	K21	DVSS	Y10	F2W_DATA
B2	CMMCLK	K23	SIM1_SIO	Y13	KPCOL2
B3	REXTDN	K24	SIM2_SRST	Y14	BSI_CLK
B4	DVSS	K25	AUD_DAT_MISO	Y15	BPI_BUS15
B5	RCKE	K26	AUD_CLK_MOSI	Y20	AVSS18_MD
B6	RCS1_B	L2	DVDD18_MIPITX	Y21	AVSS18_MD
B7	RCS0_B	L3	RDP0	Y22	EINT10
B8	RA0	L4	DVSS18_MIPITX	Y23	EINT9
B9	RA1	L10	DVSS	Y25	EINT5
B10	DVSS	L11	VCCK	Y26	DVDD18_IO1
B11	RDQ16	L12	VCCK	AA1	SCL2
B12	DVSS	L13	VCCK	AA2	SDA2
B13	RDQ18	L14	VCCK	AA3	SCL0
B14	DVSS	L15	VCCK	AA4	WB_CRTL3
B15	RDQ3	L16	VCCK	AA5	WB_CRTL2
B16	RDQ7	L17	VCCK	AA6	WB_CRTL1
B17	DVSS	L18	DVSS	AA10	F2W_CLK
B18	RDQ5	L20	SIM2_SCLK	AA13	KPROW2
B19	RDQ10	L21	SIM1_SCLK	AA14	BSI_DATA1
B20	RDQ14	L23	SIM1_SRST	AA17	BPI_BUS8
B21	RDQ8	L24	SIM2_SIO	AA18	AVSS18_AP
B22	DVSS	L25	RTC32K_CK	AA21	AVSS18_MD
B23	RDQ26	L26	DVDD18_IO0	AA23	EINT6

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Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
B24	DVSS	M1	TDP0	AA24	EINT2
B25	RDQ28	M2	TDN0	AA25	EINT8
B26	RDQ27	M3	TCP	AA26	EINT7
C2	MSDC1_DAT2	M4	TCN	AB3	SDA0
C3	MSDC1_CLK	M5	TDN3	AB4	WB_CRTL5
C4	DVSS	M7	DVSS18_MIPITX	AB5	WB_CRTL4
C6	RA8	M8	DVSS18_MIPITX	AB6	AVSS18_WBG
C7	RA5	M10	VCCK	AB8	AVSS18_WBG
C8	DVSS	M11	DVSS	AB9	SPI_MI
C10	RDQ17	M12	DVSS	AB13	KPCOL0
C11	DVSS	M13	DVSS	AB14	BSI_DATA0
C12	DVSS	M14	DVSS	AB17	BPI_BUS13
C14	RDQ0	M15	DVSS	AB19	AVSS18_AP
C15	RDQ2	M16	DVSS	AB21	AVSS18_MD
C16	DVSS	M17	DVSS	AB23	BPI_BUS1
C17	DVSS	M18	VCCK	AB24	BPI_BUS0
C18	DVSS	M20	DVSS	AB25	ANT_SEL0
C19	RDQ11	M24	SRCLKENAI	AC1	WB_RXIP
C20	DVSS	M25	SYSRSTB	AC2	WB_RXIN
C21	DVSS	N1	VRT	AC3	AVSS18_WBG
C22	DVSS	N2	TDN1	AC5	AVSS18_WBG
C23	DVSS	N3	DVSS18_MIPITX	AC7	AVSS18_WBG
C24	RDQ30	N5	TDP3	AC8	SPI_CS
C25	DVSS	N10	VCCK	AC9	SPI_MO
C26	RDQ31	N11	DVSS	AC10	EINT20
D1	DVDD18_IO2	N12	VCCK_VPROC	AC11	EINT17
D2	MSDC1_DAT1	N13	VCCK_VPROC	AC13	KPROW0
D3	MSDC1_DAT3	N14	VCCK_VPROC	AC14	BSI_DATA2
D4	DVSS	N15	VCCK_VPROC	AC15	BPI_BUS14
D5	DVSS	N16	VCCK_VPROC	AC16	BPI_BUS10
D6	RA7	N17	VCCK_VPROC	AC17	BPI_BUS12
D7	DVSS	N18	VCCK	AC19	AUX_IN0
D8	RA2	N21	DVSS	AC21	AVSS18_MD
D9	DVSS	N23	CHD_DP	AC23	BPI_BUS4
D10	RDQM2	N24	CHD_DM	AC24	BPI_BUS3
D11	DVSS	N25	SRCLKENA	AC25	ANT_SEL2
D12	RDQ20	N26	WATCHDOG	AC26	ANT_SEL1
D13	DVSS	P1	TDP2	AD2	WB_RXQP

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Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
D14	RDQ1	P2	TDP1	AD4	AVSS18_WBG
D15	DVSS	P9	VCCK	AD6	XIN_WBG
D16	RDQM0	P10	DVSS	AD7	SPI_CK
D17	DVSS	P11	DVSS	AD8	SCL1
D18	RDQM1	P12	DVSS	AD9	DISP_PWM
D20	RDQ13	P13	DVSS	AD10	EINT18
D21	DVSS	P14	VCCK_VPROC	AD13	KPCOL1
D22	RDQ15	P15	VCCK_VPROC	AD14	BSI_EN
D23	RDQM3	P16	DVSS	AD16	BPI_BUS9
D24	DVSS	P17	DVSS	AD19	AUX_IN1
D25	RDQ24	P18	VCCK	AD22	AVSS18_MD
D26	MSDC0_CLK	P21	DVSS	AD24	BPI_BUS6
E1	DVDD28_MSDC1	P22	URXD2	AD25	BPI_BUS2
E2	CMDAT0	P23	UTXD2	AD26	DVDD28_BPI
E3	MSDC1_CMD	P25	USB_VRT	AE1	WB_TXIP
E4	MSDC1_DAT0	P26	AVDD18_USB	AE2	WB_RXQN
E5	DVSS	R1	TDN2	AE3	AVSS18_WBG
E7	DVDD12_EMI	R2	DVSS	AE4	AVDD18_WBG
E8	DVSS	R4	DVDD18_EFUSE	AE5	AVSS18_WBG
E9	RCLK0	R5	FSOURCE_P	AE6	WB_SEN
E10	DVSS	R7	MSDC2_CLK	AE7	SDA1
E12	RDQS2_B	R9	VCCK	AE9	EINT19
E15	RDQS0_B	R10	VCCK	AE10	EINT16
E17	RDQS1_B	R11	DVSS	AE12	JTDO
E18	DVSS	R12	VCCK_VPROC	AE13	KPROW1
E20	RDQS3	R13	VCCK_VPROC	AE14	TXBPI
E21	DVSS	R14	VCCK_VPROC	AE18	DVDD18_PLLGP
E23	MSDC0_DAT6	R15	VCCK_VPROC	AE19	AVDD18_AP
E24	MSDC0_CMD	R16	VCCK_VPROC	AE21	AVDD18_MD
E25	MSDC0_DAT2	R17	VCCK_VPROC	AE22	AVDD28_DAC
E26	MSDC0_DAT3	R18	VCCK	AE24	APC
F2	CMDAT1	R23	URXD3	AE25	BPI_BUS5
F5	RCP_A	T23	UTXD3	AF1	WB_TXIN
F6	DVSS	R24	AVSS33_USB	AF2	WB_TXQN
F7	DVDD12_EMI	R25	USB_DM	AF3	AVSS18_WBG
F8	DVDD12_EMI	R26	USB_DP	AF4	GPS_RXIP
F9	RCLK0_B	T1	MSDC2_DAT2	AF5	GPS_RXQN
F12	RDQS2	T2	MSDC2_DAT3	AF6	WB_RSTB

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Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
F15	RDQS0	T3	MSDC2_CMD	AF7	WB_SDATA
F16	VREF	T5	MSDC2_DAT1	AF8	EINT14
F17	RDQS1	T6	MSDC2_DAT0	AF9	GPIO13
F18	DVSS	T10	VCCK	AF10	EINT11
F20	RDQS3_B	T11	DVSS	AF11	TESTMODE
F22	MSDC0_DAT7	T12	DVSS	AF12	JTCK
F24	MSDC0_DAT5	T13	DVSS	AF13	JTMS
G1	DVDD18_MIPIIO	T14	VCCK_VPROC	AF14	VM1
G2	RDP3	T15	VCCK_VPROC	AF15	BPI_BUS11
G3	RDN0_A	T16	DVSS	AF16	BPI_BUS7
G4	RDP0_A	T17	DVSS	AF17	AUX_YP
G5	RCN_A	T18	DVSS	AF18	AUX_XP
G6	DVSS	T21	DVSS	AF19	AVSS_REFN
G7	DVSS	T24	AVDD33_USB	AF20	UL_Q_N
G8	DVDD12_EMI	U2	UTXD1	AF21	UL_I_N
G9	DVDD12_EMI	U3	LCM_RST	AF22	UL_I_P
G11	DVDD12_EMI	U5	I2S_LRCK	AF25	VBIAS
G13	DVDD12_EMI	U7	AVSS18_WBG	AF26	CLK26M
G14	DVSS	U10	VCCK	AG1	AVSS18_WBG
G15	DVDD12_EMI	U11	DVSS	AG2	WB_TXQP
G16	DVDD12_EMI	U12	DVSS	AG4	GPS_RXIN
G17	DVSS	U15	VCCK_VPROC	AG5	GPS_RXQP
G18	DVDD12_EMI	U16	VCCK_VPROC	AG7	WB_SCLK
G20	DVSS	U17	AVSS18_AP	AG8	EINT15
G22	MSDC0_DAT0	U18	AVSS18_AP	AG10	GPIO12
G23	MSDC0_DAT1	U20	AVSS18_MD	AG11	JTDI
G24	MSDC0_DAT4	U21	AVSS18_MD	AG13	DVDD18_IO4
G25	MSDC0_RSTB	U24	PCM_TX	AG14	VM0
G26	DVDD18_MSDC0	U25	DVDD18_IO1	AG16	AUX_YM
H2	RDN3	V1	DVDD28_MSDC2	AG17	AUX_XM
H3	RDN1_A	V2	URXD1	AG19	REFP
H4	DVSS18_MIPIIO	V5	I2S_BCK	AG20	UL_Q_P
H5	DVSS18_MIPIIO	V7	AVSS18_WBG	AG22	DL_Q_P
H8	DVDD12_EMI	V10	VCCK	AG23	DL_Q_N
H10	DVSS	V11	DVSS	AG24	DL_I_N
H11	DVDD12_EMI	V12	DVSS	AG25	DL_I_P
H12	DVSS	V13	DVSS	AG26	AVSS18_MD
H13	DVDD12_EMI	V14	DVSS		

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Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
H14	DVSS	V15	VCCK_VPROC		
H15	DVDD12_EMI	V16	VCCK_VPROC		
H16	DVDD12_EMI	V17	AVSS18_AP		
H17	DVSS	V18	AVSS18_AP		

Table 2-2. LPDDR3 pin coordinate

Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
A1	TP_MEMPLL	H18	DVDD12_EMI	V20	AVSS18_MD
A2	AVSS18_MEMPLL	H20	DVSS	V21	AVSS18_MD
A3	AVDD18_MEMPLL	H22	PWRAP_SPI0_MO	V22	EINT1
A4	RA9	H23	PWRAP_SPI0_CK	V23	PCM_CLK
A5	RA13	H24	PWRAP_INT	V24	EINT3
A7	RA2	J1	RDP2	V25	PCM_SYNC
A8	RA0	J2	RDN2	V26	PCM_RX
A10	RA4	J3	RDP1_A	W1	DVDD18_IO3
A11	RA11	J5	DVSS18_MIPIIO	W2	URXD0
A13	RA15	J7	DVSS18_MIPIIO	W5	I2S_DATA_IN
A14	RA10	J21	DVSS	W7	AVSS18_WBG
A16	RODT0_R	J23	PWRAP_SPI0_CSN	W20	AVSS18_MD
A19	DVSS	J24	PWRAP_SPI0_MI	W21	AVSS18_MD
A20	RDQ7	J25	AUD_DAT_MOSI	W22	EINT0
A22	RDQ0	K1	RDP1	W25	EINT4
A23	RDQ8	K2	RDN1	Y2	UTXD0
A25	RDQ12	K3	RDN0	Y3	DSI_TE
A26	DVSS	K5	RCN	Y6	WB_CRTL0
B1	CMPCLK	K6	RCP	Y7	AVSS18_WBG
B2	CMMCLK	K21	DVSS	Y10	F2W_DATA
B3	REXTDN	K23	SIM1_SIO	Y13	KPCOL2
B4	DVSS	K24	SIM2_SRST	Y14	BSI_CLK
B5	RCKE	K25	AUD_DAT_MISO	Y15	BPI_BUS15
B6	RCS1_B	K26	AUD_CLK_MOSI	Y20	AVSS18_MD
B7	RCS0_B	L2	DVDD18_MIPITX	Y21	AVSS18_MD
B8	RA8	L3	RDP0	Y22	EINT10
B9	RA6	L4	DVSS18_MIPITX	Y23	EINT9
B10	DVSS	L10	DVSS	Y25	EINT5
B11	RA12	L11	VCCK	Y26	DVDD18_IO1

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Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
B12	DVSS	L12	VCCK	AA1	SCL2
B13	RBA1	L13	VCCK	AA2	SDA2
B14	DVSS	L14	VCCK	AA3	SCL0
B15	RA3	L15	VCCK	AA4	WB_CRTL3
B16	RBA2	L16	VCCK	AA5	WB_CRTL2
B17	DVSS	L17	VCCK	AA6	WB_CRTL1
B19	RDQ5	L18	DVSS	AA10	F2W_CLK
B20	RDQ3	L20	SIM2_SCLK	AA13	KPROW2
B21	RDQ1	L21	SIM1_SCLK	AA14	BSI_DATA1
B22	DVSS	L23	SIM1_SRST	AA17	BPI_BUS8
B23	RDQ10	L24	SIM2_SIO	AA18	AVSS18_AP
B24	DVSS	L25	RTC32K_CK	AA21	AVSS18_MD
B25	RDQ14	L26	DVDD18_IO0	AA23	EINT6
B26	RDQ15	M1	TDP0	AA24	EINT2
C2	MSDC1_DAT2	M2	TDN0	AA25	EINT8
C3	MSDC1_CLK	M3	TCP	AA26	EINT7
C4	DVSS	M4	TCN	AB3	SDA0
C6	RRESET_B	M5	TDN3	AB4	WB_CRTL5
C7	RA5	M7	DVSS18_MIPITX	AB5	WB_CRTL4
C8	DVSS	M8	DVSS18_MIPITX	AB6	AVSS18_WBG
C10	RA14	M10	VCCK	AB8	AVSS18_WBG
C11	DVSS	M11	DVSS	AB9	SPI_MI
C12	DVSS	M12	DVSS	AB13	KPCOL0
C14	RRAS_B	M13	DVSS	AB14	BSI_DATA0
C15	RCAS_B	M14	DVSS	AB17	BPI_BUS13
C16	DVSS	M15	DVSS	AB19	AVSS18_AP
C17	DVSS	M16	DVSS	AB21	AVSS18_MD
C18	DVSS	M17	DVSS	AB23	BPI_BUS1
C19	RDQ4	M18	VCCK	AB24	BPI_BUS0
C20	DVSS	M20	DVSS	AB25	ANT_SEL0
C21	DVSS	M24	SRCLKENAI	AC1	WB_RXIP
C22	DVSS	M25	SYSRSTB	AC2	WB_RXIN
C23	DVSS	N1	VRT	AC3	AVSS18_WBG
C24	RDQ9	N2	TDN1	AC5	AVSS18_WBG
C25	DVSS	N3	DVSS18_MIPITX	AC7	AVSS18_WBG
C26	RDQ13	N5	TDP3	AC8	SPI_CS
D1	DVDD18_IO2	N10	VCCK	AC9	SPI_MO
D2	MSDC1_DAT1	N11	DVSS	AC10	EINT20

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Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
D3	MSDC1_DAT3	N12	VCCK_VPROC	AC11	EINT17
D4	DVSS	N13	VCCK_VPROC	AC13	KPROW0
D5	DVSS	N14	VCCK_VPROC	AC14	BSI_DATA2
D6	RA7	N15	VCCK_VPROC	AC15	BPI_BUS14
D7	DVSS	N16	VCCK_VPROC	AC16	BPI_BUS10
D8	RBA0	N17	VCCK_VPROC	AC17	BPI_BUS12
D9	DVSS	N18	VCCK	AC19	AUX_IN0
D11	DVSS	N21	DVSS	AC21	AVSS18_MD
D12	RA1	N23	CHD_DP	AC23	BPI_BUS4
D13	DVSS	N24	CHD_DM	AC24	BPI_BUS3
D14	RWR_B	N25	SRCLKENA	AC25	ANT_SEL2
D15	DVSS	N26	WATCHDOG	AC26	ANT_SEL1
D17	DVSS	P1	TDP2	AD2	WB_RXQP
D18	RDQM0	P2	TDP1	AD4	AVSS18_WBG
D20	RDQ6	P9	VCCK	AD6	XIN_WBG
D21	DVSS	P10	DVSS	AD7	SPI_CK
D22	RDQ2	P11	DVSS	AD8	SCL1
D23	RDQM1	P12	DVSS	AD9	DISP_PWM
D24	DVSS	P13	DVSS	AD10	EINT18
D25	RDQ11	P14	VCCK_VPROC	AD13	KPCOL1
D26	MSDC0_CLK	P15	VCCK_VPROC	AD14	BSI_EN
E1	DVDD28_MSDC1	P16	DVSS	AD16	BPI_BUS9
E2	CMDAT0	P17	DVSS	AD19	AUX_IN1
E3	MSDC1_CMD	P18	VCCK	AD22	AVSS18_MD
E4	MSDC1_DAT0	P21	DVSS	AD24	BPI_BUS6
E5	DVSS	P22	URXD2	AD25	BPI_BUS2
E7	DVDD12_EMI	P23	UTXD2	AD26	DVDD28_BPI
E8	DVSS	P25	USB_VRT	AE1	WB_TXIP
E9	RCLK0	P26	AVDD18_USB	AE2	WB_RXQN
E10	DVSS	R1	TDN2	AE3	AVSS18_WBG
E17	RDQS0_B	R2	DVSS	AE4	AVDD18_WBG
E18	DVSS	R4	DVDD18_EFUSE	AE5	AVSS18_WBG
E20	RDQS1	R5	FSOURCE_P	AE6	WB_SEN
E21	DVSS	R7	MSDC2_CLK	AE7	SDA1
E23	MSDC0_DAT6	R9	VCCK	AE9	EINT19
E24	MSDC0_CMD	R10	VCCK	AE10	EINT16
E25	MSDC0_DAT2	R11	DVSS	AE12	JTDO
E26	MSDC0_DAT3	R12	VCCK_VPROC	AE13	KPROW1

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Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
F2	CMDAT1	R13	VCCK_VPROC	AE14	TXBPI
F5	RCP_A	R14	VCCK_VPROC	AE18	DVDD18_PLLGP
F6	DVSS	R15	VCCK_VPROC	AE19	AVDD18_AP
F7	DVDD12_EMI	R16	VCCK_VPROC	AE21	AVDD18_MD
F8	DVDD12_EMI	R17	VCCK_VPROC	AE22	AVDD28_DAC
F9	RCLK0_B	R18	VCCK	AE24	APC
F16	VREF	R23	URXD3	AE25	BPI_BUS5
F17	RDQS0	R24	AVSS33_USB	AF1	WB_TXIN
F18	DVSS	R25	USB_DM	AF2	WB_TXQN
F20	RDQS1_B	R26	USB_DP	AF3	AVSS18_WBG
F22	MSDC0_DAT7	T1	MSDC2_DAT2	AF4	GPS_RXIP
F24	MSDC0_DAT5	T2	MSDC2_DAT3	AF5	GPS_RXQN
G1	DVDD18_MIPIIO	T3	MSDC2_CMD	AF6	WB_RSTB
G2	RDP3	T5	MSDC2_DAT1	AF7	WB_SDATA
G3	RDN0_A	T6	MSDC2_DAT0	AF8	EINT14
G4	RDP0_A	T10	VCCK	AF9	GPIO13
G5	RCN_A	T11	DVSS	AF10	EINT11
G6	DVSS	T12	DVSS	AF11	TESTMODE
G7	DVSS	T13	DVSS	AF12	JTCK
G8	DVDD12_EMI	T14	VCCK_VPROC	AF13	JTMS
G9	DVDD12_EMI	T15	VCCK_VPROC	AF14	VM1
G11	DVDD12_EMI	T16	DVSS	AF15	BPI_BUS11
G13	DVDD12_EMI	T17	DVSS	AF16	BPI_BUS7
G14	DVSS	T18	DVSS	AF17	AUX_YP
G15	DVDD12_EMI	T21	DVSS	AF18	AUX_XP
G16	DVDD12_EMI	T23	UTXD3	AF19	AVSS_REFN
G17	DVSS	T24	AVDD33_USB	AF20	UL_Q_N
G18	DVDD12_EMI	U2	UTXD1	AF21	UL_I_N
G20	DVSS	U3	LCM_RST	AF22	UL_I_P
G22	MSDC0_DAT0	U5	I2S_LRCK	AF25	VBIAS
G23	MSDC0_DAT1	U7	AVSS18_WBG	AF26	CLK26M
G24	MSDC0_DAT4	U10	VCCK	AG1	AVSS18_WBG
G25	MSDC0_RSTB	U11	DVSS	AG2	WB_TXQP
G26	DVDD18_MSDC0	U12	DVSS	AG4	GPS_RXIN
H2	RDN3	U15	VCCK_VPROC	AG5	GPS_RXQP
H3	RDN1_A	U16	VCCK_VPROC	AG7	WB_SCLK
H4	DVSS18_MIPIIO	U17	AVSS18_AP	AG8	EINT15
H5	DVSS18_MIPIIO	U18	AVSS18_AP	AG10	GPIO12

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Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
H8	DVDD12_EMI	U20	AVSS18_MD	AG11	JTDI
H10	DVSS	U21	AVSS18_MD	AG13	DVDD18_IO4
H11	DVDD12_EMI	U24	PCM_TX	AG14	VM0
H12	DVSS	U25	DVDD18_IO1	AG16	AUX_YM
H13	DVDD12_EMI	V1	DVDD28_MSDC2	AG17	AUX_XM
H14	DVSS	V2	URXD1	AG19	REFP
H15	DVDD12_EMI	V5	I2S_BCK	AG20	UL_Q_P
H16	DVDD12_EMI	V7	AVSS18_WBG	AG22	DL_Q_P
H17	DVSS	V10	VCCK	AG23	DL_Q_N
A1	TP_MEMPLL	V11	DVSS	AG24	DL_I_N
A2	AVSS18_MEMPLL	V12	DVSS	AG25	DL_I_P
A3	AVDD18_MEMPLL	V13	DVSS	AG26	AVSS18_MD
A4	RA9	V14	DVSS		
A5	RA13	V15	VCCK_VPROC		
A7	RA2	V16	VCCK_VPROC		
A8	RA0	V17	AVSS18_AP		
A10	RA4	V18	AVSS18_AP		

2.1.2 Detailed Pin Description

Table 2-3. Acronym for pin type

Abbreviation	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-direction
DI	Digital input
DO	Digital output
DIO	Digital bi-direction
P	Power
G	Ground

Table 2-4. Detailed pin description

Pin name	Type	Description	Power domain
SYSTEM			
SYSRSTB	DIO	System reset input	DVDD18_IO0
WATCHDOG	DO	Watchdog reset output	DVDD18_IO0
TESTMODE	DIO	Test mode	DVDD18_IO4
RTC32K_CK	DIO	32K clock input	DVDD18_IO0

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Pin name	Type	Description	Power domain
SRCLKENAI	DIO	26MHz co-clock enable input	DVDD18_IO0
SRCLKENA	DIO	26MHz co-clock enable output	DVDD18_IO0
PMIC			
PWRAP_SPI0_MO	DIO	PMIC SPI control interface	DVDD18_IO0
PWRAP_SPI0_MI	DIO	PMIC SPI control interface	DVDD18_IO0
PWRAP_SPI0_CSN	DIO	PMIC SPI control interface	DVDD18_IO0
PWRAP_SPI0_CLK	DIO	PMIC SPI control interface	DVDD18_IO0
PWRAP_INT	DIO	PMIC SPI control interface	DVDD18_IO0
AUD_CLK_MOSI	DIO	PMIC audio input interface	DVDD18_IO0
AUD_DAT_MOSI	DIO	PMIC audio input interface	DVDD18_IO0
AUD_DAT_MISO	DIO	PMIC audio input interface	DVDD18_IO0
SIM			
SIM1_SIO	DIO	SIM1 data, PMIC interface	DVDD18_IO0
SIM1_SRST	DIO	SIM1 reset, PMIC interface	DVDD18_IO0
SIM1_SCLK	DIO	SIM1 clock, PMIC interface	DVDD18_IO0
SIM2_SIO	DIO	SIM2 data, PMIC interface	DVDD18_IO0
SIM2_SRST	DIO	SIM2 reset, PMIC interface	DVDD18_IO0
SIM2_SCLK	DIO	SIM2 clock, PMIC interface	DVDD18_IO0
JTAG			
JTCK	DIO	JTCK	DVDD18_IO4
JTDO	DIO	JTDO	DVDD18_IO4
JTDI	DIO	JTDI	DVDD18_IO4
JTMS	DIO	JTMS	DVDD18_IO4
LCD			
DISP_PWM	DIO	Display PWM output	DVDD18_IO4
DSI_TE	DIO	Parallel display interface tearing effect	DVDD18_IO3
LCM_RST	DIO	Parallel display interface reset signal	DVDD18_IO3
I2S			
I2S_DATA_IN	DIO	I2S data input pin	DVDD18_IO3
I2S_BCK	DIO	I2S clock	DVDD18_IO3
I2S_LRCK	DIO	I2S word select	DVDD18_IO3
PCM/I2S merge interface			
PCM_TX	DIO	PCM audio interface	DVDD18_IO1
PCM_CLK	DIO	PCM audio interface	DVDD18_IO1
PCM_RX	DIO	PCM audio interface	DVDD18_IO1
PCM_SYNC	DIO	PCM audio interface	DVDD18_IO1
EINT			
EINT0	DIO	External interrupt 0	DVDD18_IO1
EINT1	DIO	External interrupt 1	DVDD18_IO1
EINT2	DIO	External interrupt 2	DVDD18_IO1
EINT3	DIO	External interrupt 3	DVDD18_IO1
EINT4	DIO	External interrupt 4	DVDD18_IO1
EINT5	DIO	External interrupt 5	DVDD18_IO1

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Pin name	Type	Description	Power domain
EINT6	DIO	External interrupt 6	DVDD18_IO1
EINT7	DIO	External interrupt 7	DVDD18_IO1
EINT8	DIO	External interrupt 8	DVDD18_IO1
EINT9	DIO	External interrupt 9	DVDD18_IO1
EINT10	DIO	External interrupt 10	DVDD18_IO1
EINT11	DIO	External interrupt 11	DVDD18_IO4
EINT14	DIO	External interrupt 14	DVDD18_IO4
EINT15	DIO	External interrupt 15	DVDD18_IO4
EINT16	DIO	External interrupt 16	DVDD18_IO4
EINT17	DIO	External interrupt 17	DVDD18_IO4
EINT18	DIO	External interrupt 18	DVDD18_IO4
EINT19	DIO	External interrupt 18	DVDD18_IO4
EINT20	DIO	External interrupt 20	DVDD18_IO4
GPIO			
GPIO12	DIO	GPIO12	DVDD18_IO4
GPIO13	DIO	GPIO12	DVDD18_IO4
UART			
URXD0	DIO	UART0 RX	DVDD18_IO3
UTXD0	DIO	UART0 TX	DVDD18_IO3
URXD1	DIO	UART1 RX	DVDD18_IO3
UTXD1	DIO	UART1 TX	DVDD18_IO3
URXD2	DIO	UART2 RX	DVDD18_IO1
UTXD2	DIO	UART2 TX	DVDD18_IO1
URXD3	DIO	UART3 RX	DVDD18_IO1
UTXD3	DIO	UART3 TX	DVDD18_IO1
SPI			
SPI_CSN	DIO	SPI chip select	DVDD18_IO4
SPI_MI	DIO	SPI data in	DVDD18_IO4
SPI_MO	DIO	SPI data out	DVDD18_IO4
SPI_CLK	DIO	SPI clock	DVDD18_IO4
BPI			
BPI_BUS0	DIO	BPI1 BUS0	DVDD28_BPI/DVDD18_IO1
BPI_BUS1	DIO	BPI1 BUS1	DVDD28_BPI/DVDD18_IO1
BPI_BUS2	DIO	BPI1 BUS2	DVDD28_BPI/DVDD18_IO1
BPI_BUS3	DIO	BPI1 BUS3	DVDD28_BPI/DVDD18_IO1
BPI_BUS4	DIO	BPI1 BUS4	DVDD28_BPI/DVDD18_IO1
BPI_BUS5	DIO	BPI1 BUS5	DVDD28_BPI/DVDD18_IO1
BPI_BUS6	DIO	BPI1 BUS6	DVDD28_BPI/DVDD18_IO1
BPI_BUS7	DIO	BPI1 BUS7	DVDD18_IO4
BPI_BUS8	DIO	BPI1 BUS8	DVDD18_IO4
BPI_BUS9	DIO	BPI1 BUS9	DVDD18_IO4
BPI_BUS10	DIO	BPI1 BUS10	DVDD18_IO4
BPI_BUS11	DIO	BPI1 BUS11	DVDD18_IO4

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Pin name	Type	Description	Power domain
BPI_BUS12	DIO	BPI1 BUS12	DVDD18_IO4
BPI_BUS13	DIO	BPI1 BUS13	DVDD18_IO4
BPI_BUS14	DIO	BPI1 BUS14	DVDD18_IO4
BPI_BUS15	DIO	BPI1 BUS15	DVDD18_IO4
ANT_SEL0	DIO	Antenna select 0	DVDD28_BPI/DVDD18_IO1
ANT_SEL1	DIO	Antenna select 1	DVDD28_BPI/DVDD18_IO1
ANT_SEL2	DIO	Antenna select 2	DVDD28_BPI/DVDD18_IO1
VM			
VM1	DIO	PA mode selection	DVDD28_BPI/DVDD18_IO1
VM0	DIO	PA mode selection	DVDD28_BPI/DVDD18_IO1
BSI			
BSI_CS0	DIO	BSI CS0	DVDD18_IO4
BSI_CLK	DIO	BSI CLK	DVDD18_IO4
BSI_DATA0	DIO	BSI DATA0	DVDD18_IO4
BSI_DATA1	DIO	BSI DATA1	DVDD18_IO4
BSI_DATA2	DIO	BSI DATA2	DVDD18_IO4
TXBPI	DIO	RF MT6166 TXBPI	DVDD18_IO4
MSDC0			
MSDC0_DAT7	DIO	MSDC0 data7 pin	DVDD18_MSDC0
MSDC0_DAT6	DIO	MSDC0 data6 pin	DVDD18_MSDC0
MSDC0_DAT5	DIO	MSDC0 data5 pin	DVDD18_MSDC0
MSDC0_RSTB	DIO	MSDC0 reset output	DVDD18_MSDC0
MSDC0_DAT4	DIO	MSDC0 data4 pin	DVDD18_MSDC0
MSDC0_DAT2	DIO	MSDC0 data2 pin	DVDD18_MSDC0
MSDC0_DAT3	DIO	MSDC0 data3 pin	DVDD18_MSDC0
MSDC0_CMD	DIO	MSDC0 command pin	DVDD18_MSDC0
MSDC0_CLK	DIO	MSDC0 clock output	DVDD18_MSDC0
MSDC0_DAT1	DIO	MSDC0 data1 pin	DVDD18_MSDC0
MSDC0_DAT0	DIO	MSDC0 data0 pin	DVDD18_MSDC0
MSDC1			
MSDC1_CLK	DIO	MSDC1 clock output	DVDD28_MSDC1/DVDD18_IO2
MSDC1_CMD	DIO	MSDC1 command pin	DVDD28_MSDC1/DVDD18_IO2
MSDC1_DAT0	DIO	MSDC1 data0 pin	DVDD28_MSDC1/DVDD18_IO2
MSDC1_DAT1	DIO	MSDC1 data1 pin	DVDD28_MSDC1/DVDD18_IO2
MSDC1_DAT2	DIO	MSDC1 data2 pin	DVDD28_MSDC1/DVDD18_IO2
MSDC1_DAT3	DIO	MSDC1 data3 pin	DVDD28_MSDC1/DVDD18_IO2
MSDC2			
MSDC2_CLK	DIO	MSDC2 clock output	DVDD28_MSDC2/DVDD18_IO3
MSDC2_CMD	DIO	MSDC2 command pin	DVDD28_MSDC2/DVDD18_IO3
MSDC2_DAT0	DIO	MSDC2 data0 pin	DVDD28_MSDC2/DVDD18_IO3
MSDC2_DAT1	DIO	MSDC2 data1 pin	DVDD28_MSDC2/DVDD18_IO3
MSDC2_DAT2	DIO	MSDC2 data2 pin	DVDD28_MSDC2/DVDD18_IO3
MSDC2_DAT3	DIO	MSDC2 data3 pin	DVDD28_MSDC2/DVDD18_IO3

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Pin name	Type	Description	Power domain
WiFi/BT/GPS			
WB_SDATA	DIO	SPI control data	DVDD18_IO4
WB_SCLK	DIO	SPI control clock	DVDD18_IO4
WB_SEN	DIO	SPI control enable	DVDD18_IO4
F2W_CLK	DIO	FM clock	DVDD18_IO4
F2W_DATA	DIO	FM data	DVDD18_IO4
WB_CRTL0	DIO	Data bus 0	DVDD18_IO3
WB_CRTL1	DIO	Data bus 1	DVDD18_IO3
WB_CRTL2	DIO	Data bus 2	DVDD18_IO3
WB_CRTL3	DIO	Data bus 3	DVDD18_IO3
WB_CRTL4	DIO	Data bus 4	DVDD18_IO3
WB_CRTL5	DIO	Data bus 5	DVDD18_IO3
EFUSE			
FSOURCE_P	DIO	E-FUSE blowing power control	FSOURCE_P
EMI			
RCLK0	DIO	DRAM clock 0 output	DVDD12_EMI
RCLK0_B	DIO	DRAM clock 0 output #	DVDD12_EMI
RCLK1	DIO	DRAM clock 1 output	DVDD12_EMI
RCLK1_B	DIO	DRAM clock 1 output #	DVDD12_EMI
RCKE	DIO	DRAM command output CKE	DVDD12_EMI
RCS0_B	DIO	DRAM chip select 0 #	DVDD12_EMI
RCS1_B	DIO	DRAM chip select 1 #	DVDD12_EMI
RA0	DIO	DRAM address output 0	DVDD12_EMI
RA1	DIO	DRAM address output 1	DVDD12_EMI
RA2	DIO	DRAM address output 2	DVDD12_EMI
RA3	DIO	DRAM address output 3	DVDD12_EMI
RA4	DIO	DRAM address output 4	DVDD12_EMI
RA5	DIO	DRAM address output 5	DVDD12_EMI
RA6	DIO	DRAM address output 6	DVDD12_EMI
RA7	DIO	DRAM address output 7	DVDD12_EMI
RA8	DIO	DRAM address output 8	DVDD12_EMI
RA9	DIO	DRAM address output 9	DVDD12_EMI
RDQM0	DIO	DRAM DQM 0	DVDD12_EMI
RDQM1	DIO	DRAM DQM 1	DVDD12_EMI
RDQM2	DIO	DRAM DQM 2	DVDD12_EMI
RDQM3	DIO	DRAM DQM 3	DVDD12_EMI
RDQS0	DIO	DRAM DQS 0	DVDD12_EMI
RDQS0_B	DIO	DRAM DQS 0 #	DVDD12_EMI
RDQS1	DIO	DRAM DQS 1	DVDD12_EMI
RDQS1_B	DIO	DRAM DQS 1 #	DVDD12_EMI
RDQS2	DIO	DRAM DQS 2	DVDD12_EMI
RDQS2_B	DIO	DRAM DQS 2 #	DVDD12_EMI
RDQS3	DIO	DRAM DQS 3	DVDD12_EMI

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Pin name	Type	Description	Power domain
RDQS3_B	DIO	DRAM DQS 3 #	DVDD12_EMI
RDQ0	DIO	DRAM data pin 0	DVDD12_EMI
RDQ1	DIO	DRAM data pin 1	DVDD12_EMI
RDQ2	DIO	DRAM data pin 2	DVDD12_EMI
RDQ3	DIO	DRAM data pin 3	DVDD12_EMI
RDQ4	DIO	DRAM data pin 4	DVDD12_EMI
RDQ5	DIO	DRAM data pin 5	DVDD12_EMI
RDQ6	DIO	DRAM data pin 6	DVDD12_EMI
RDQ7	DIO	DRAM data pin 7	DVDD12_EMI
RDQ8	DIO	DRAM data pin 8	DVDD12_EMI
RDQ9	DIO	DRAM data pin 9	DVDD12_EMI
RDQ10	DIO	DRAM data pin 10	DVDD12_EMI
RDQ11	DIO	DRAM data pin 11	DVDD12_EMI
RDQ12	DIO	DRAM data pin 12	DVDD12_EMI
RDQ13	DIO	DRAM data pin 13	DVDD12_EMI
RDQ14	DIO	DRAM data pin 14	DVDD12_EMI
RDQ15	DIO	DRAM data pin 15	DVDD12_EMI
RDQ16	DIO	DRAM data pin 16	DVDD12_EMI
RDQ17	DIO	DRAM data pin 17	DVDD12_EMI
RDQ18	DIO	DRAM data pin 18	DVDD12_EMI
RDQ19	DIO	DRAM data pin 19	DVDD12_EMI
RDQ20	DIO	DRAM data pin 20	DVDD12_EMI
RDQ21	DIO	DRAM data pin 21	DVDD12_EMI
RDQ22	DIO	DRAM data pin 22	DVDD12_EMI
RDQ23	DIO	DRAM data pin 23	DVDD12_EMI
RDQ24	DIO	DRAM data pin 24	DVDD12_EMI
RDQ25	DIO	DRAM data pin 25	DVDD12_EMI
RDQ26	DIO	DRAM data pin 26	DVDD12_EMI
RDQ27	DIO	DRAM data pin 27	DVDD12_EMI
RDQ28	DIO	DRAM data pin 28	DVDD12_EMI
RDQ29	DIO	DRAM data pin 29	DVDD12_EMI
RDQ30	DIO	DRAM data pin 30	DVDD12_EMI
RDQ31	DIO	DRAM data pin 31	DVDD12_EMI
REXTDN	DIO	DRAM REXTDN pin	DVDD12_EMI
VREF	DIO	DRAM VREF pin	DVDD12_EMI
CAM			
CMPCLK	DIO	Pixel clock from sensor	DVDD18_IO2
CMMCLK	DIO	Master clock to sensor	DVDD18_IO2
CMDAT0	DIO	CAM sensor Data0	DVDD18_IO2
CMDAT1	DIO	CAM sensor Data1	DVDD18_IO2
I2C0			
SCL0	DIO	I2C0 clock	DVDD18_IO1
SDA0	DIO	I2C0 data	DVDD18_IO1

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Pin name	Type	Description	Power domain
I2C1			
SCL1	DIO	I2C1 clock	DVDD18_IO4
SDA1	DIO	I2C1 data	DVDD18_IO4
I2C2			
SCL2	DIO	I2C2 clock	DVDD18_IO1
SDA2	DIO	I2C2 data	DVDD18_IO1
ABB			
UL_Q_N	AIO	UMTS uplink for UMTSTX_QN	AVDD18_MD
UL_Q_P	AIO	UMTS uplink for UMTSTX_QP	AVDD18_MD
UL_I_P	AIO	UMTS uplink for UMTSTX_IP	AVDD18_MD
UL_I_N	AIO	UMTS uplink for UMTSTX_IN	AVDD18_MD
VBIAS	AIO	3G PA analog control	AVDD28_DAC
APC	AIO	Automatic power control	AVDD28_DAC
CLK26M	AIO	26MHz clock input for AP & 1st modem	AVDD18_MD
DL_Q_P	AIO	UMTS uplink for UMTSRX_QP	AVDD18_MD
DL_Q_N	AIO	UMTS uplink for UMTSRX_QN	AVDD18_MD
DL_I_N	AIO	UMTS uplink for UMTSRX_IN	AVDD18_MD
DL_I_P	AIO	UMTS uplink for UMTSRX_IP	AVDD18_MD
REFN	AIO	Negative reference port for internal circuit	AVDD18_AP
REFP	AIO	Positive reference port for internal circuit	AVDD18_AP
AUX_IN0	AIO	AuxADC external input channel 0	AVDD18_AP
AUX_IN1	AIO	AuxADC external input channel 1	AVDD18_AP
AUX_XP	AIO	AuxADC channel for touch screen TP_X+	AVDD18_AP
AUX_YP	AIO	AuxADC channel for touch screen TP_Y+	AVDD18_AP
AUX_XM	AIO	AuxADC channel for touch screen TP_X-	AVDD18_AP
AUX_YM	AIO	AuxADC channel for touch screen TP_Y-	AVDD18_AP
WBG			
XIN_WB	AIO	WiFi/BT clock source	AVDD18_WBG
GPS_RXQN	AIO	RXQN for GPS	AVDD18_WBG
GPS_RXQP	AIO	RXQP for GPS	AVDD18_WBG
GPS_RXIN	AIO	RXIN for GPS	AVDD18_WBG
GPS_RXIP	AIO	RXIP for GPS	AVDD18_WBG
WB_TXQN	AIO	TXQN for WiFi/BT	AVDD18_WBG
WB_TXQP	AIO	TXQN for WiFi/BT	AVDD18_WBG
WB_TXIN	AIO	TXIN for WiFi/BT	AVDD18_WBG
WB_TXIP	AIO	TXIP for WiFi/BT	AVDD18_WBG
WB_RXQN	AIO	RXQN for WiFi/BT	AVDD18_WBG
WB_RXQP	AIO	RXQP for WiFi/BT	AVDD18_WBG
WB_RXIN	AIO	RXIN for WiFi/BT	AVDD18_WBG
WB_RXIP	AIO	RXIP for WiFi/BT	AVDD18_WBG
MIPI			
TDN3	AIO	DSI0 lane3 N	DVDD18_MIPITX
TDP3	AIO	DSI0 lane3 P	DVDD18_MIPITX
TDN2	AIO	DSI0 lane2 N	DVDD18_MIPITX

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Pin name	Type	Description	Power domain
TDP2	AIO	DSI0 lane2 P	DVDD18_MIPITX
TCN	AIO	DSI0 CK lane N	DVDD18_MIPITX
TCP	AIO	DSI0 CK lane P	DVDD18_MIPITX
TDN1	AIO	DSI0 lane1 N	DVDD18_MIPITX
TDP1	AIO	DSI0 lane1 P	DVDD18_MIPITX
TDN0	AIO	DSI0 lane0 N	DVDD18_MIPITX
TDP0	AIO	DSI0 lane0 P	DVDD18_MIPITX
VRT	AO	External resistor for DSI bias Connect 1.5K ohm 1% resistor to ground	DVDD18_MIPITX
RDN3	AIO	CSI0 lane3 N	DVDD18_MIPIRX
RDP3	AIO	CSI0 lane3 P	DVDD18_MIPIRX
RDN2	AIO	CSI0 lane2 N	DVDD18_MIPIRX
RDP2	AIO	CSI0 lane2 P	DVDD18_MIPIRX
RCN	AIO	CSI0 CK lane N	DVDD18_MIPIRX
RCP	AIO	CSI0 CK lane P	DVDD18_MIPIRX
RDN1	AIO	CSI0 lane1 N	DVDD18_MIPIRX
RDP1	AIO	CSI0 lane1 P	DVDD18_MIPIRX
RDN0	AIO	CSI0 lane0 N	DVDD18_MIPIRX
RDP0	AIO	CSI0 lane0 P	DVDD18_MIPIRX
RDN1_A	AIO	CSI1 lane1 N/Pixel data [6] from sensor	DVDD18_MIPIIO
RDP1_A	AIO	CSI1 lane1 P/Pixel data [7] from sensor	DVDD18_MIPIIO
RCN_A	AIO	CSI1 CK lane N/Pixel data [8] from sensor	DVDD18_MIPIIO
RCP_A	AIO	CSI1 CK lane P/Pixel data [9] from sensor	DVDD18_MIPIIO
RDN0_A	AIO	CSI1 lane0 N/HREF from sensor	DVDD18_MIPIIO
RDP0_A	AIO	CSI1 lane0 P/VREF from sensor	DVDD18_MIPIIO
USB			
USB_DP	AIO	USB port0 D+ differential data line	AVDD33_USB
USB_DM	AIO	USB port0 D- differential data line	AVDD33_USB
CHD_DP	AIO	BC1.1 Charger DP	AVDD33_USB
CHD_DM	AIO	BC1.1 Charger DM	AVDD33_USB
USB_VRT	AO	USB output for bias current; connect with 5.11K 1% Ohm to GND	AVDD18_USB
MEMPLL			
TP_MEMPLL	AIO	MEMPLL differential output P for debugging	AVDD18_MEMPLL
Analog power			
DVDD18_PLLGP	P	Analog power input 1.8V for PLL	-
AVDD18_AP	P	Analog power input 1.8V for AuxADC, TSENSE	-
AVDD18_MD	P	Analog power input 1.8V for BBTX, BBRX	-
AVDD18_MEMPLL	P	Analog power for MEMPLL	-
AVDD18_USB	P	Analog power 1.8V for USB	-
AVDD18_WBG	P	Analog power 1.8V for WiFi/BT/GPS	-
DVDD18_MIPITX	P	Analog power for MIPI DSI	-
DVDD18_MIPIIO	P	Analog power for MIPI CSI	-

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Pin name	Type	Description	Power domain
AVDD28_DAC	P	Analog power input 2.8V for APC	-
AVDD33_USB	P	Analog power 3.3V for USB port 1	-
Digital power			
DVDD18_IO0	P	Digital power input for IO	-
DVDD18_IO1	P	Digital power input for IO	-
DVDD18_IO2	P	Digital power input for IO	-
DVDD18_IO3	P	Digital power input for IO	-
DVDD18_IO4	P	Digital power input for IO	-
DVDD18_EFUSE	P	Digital power input for efuse IO	-
DVDD18_MSDC0	P	Digital power input for MSDC0 IO	-
DVDD28_BPI	P	Digital power input for 2.8V BPI IO	-
DVDD28_MSDC1	P	Digital power input for 1.8/3.3V MSDC IO	-
DVDD28_MSDC2	P	Digital power input for 1.8/3.3V MSDC IO	-
DVDD12_EMI	P	Digital power input for 1.2V EMI	-
VCCK	P	Digital power input for core	-
VCCK_VPROC	P	Digital power input for processor	-
Analog ground			
AVSS18_AP	G	Analog ground for AuxADC, TSENSE	-
AVSS18_MD	G	Analog ground for BBTX, BBRX	-
AVSS18_MEMPLL	G	Analog ground for MEMPLL	-
AVSS18_WBG	G	Analog ground for WiFi/BT/GPS	-
AVSS_REFN	G	Analog ground for REFN	-
AVSS33_USB	G	Analog ground for USB	-
DVSS18_MIPITX	G	Analog ground for MIPI TX	-
DVSS18_MIPIIO	G	Analog ground for MIPI IO	-
AVSS33_USB	G	Analog ground for USB	-
Digital ground			
DVSS	G	Digital ground	-

2.2 Electrical Characteristic

2.2.1 Absolute Maximum Ratings

Table 2-5. Absolute maximum ratings for power supply

Symbol or Pin name	Description	Min.	Max.	Unit
DVDD18_PLLGP	Analog power input 1.8V for PLL	1.7	1.9	V
AVDD18_AP	Analog power input 1.8V for AuxADC, TSENSE	1.7	1.9	V
AVDD18_MD	Analog power input 1.8V for BBTX, BBRX	1.7	1.9	V
AVDD28_DAC	Analog power input 2.8V for APC	2.66	2.94	V
DVDD18_MIPITX	Analog power for MIPI DSI	1.7	1.9	V
DVDD18_MIPIIO	Analog power for MIPI CSI	1.7	1.9	V

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Symbol or Pin name	Description	Min.	Max.	Unit
AVDD33_USB	Analog power 3.3V for USB	3.135	3.465	V
AVDD18_USB	Analog power 1.8V for USB	1.7	1.9	V
AVDD18_MEMPLL	Analog power for MEMPLL	1.7	1.9	V
AVDD18_WBG	Analog power for WiFi/BT/GPS	1.7	1.9	V
DVDD18_MSDC0	Digital power input for MSDC0 IO	1.7	1.95	V
DVDD18_IO0	Digital power input for IO	1.7	1.9	V
DVDD18_IO1	Digital power input for IO	1.7	1.9	V
DVDD18_IO2	Digital power input for IO	1.7	1.9	V
DVDD18_IO3	Digital power input for IO	1.7	1.9	V
DVDD18_IO4	Digital power input for IO	1.7	1.9	V
DVDD18_EFUSE	Digital power input for efuse IO	1.8	2.0	V
DVDD28_BPI	Digital power input for BPI	1.7	3.6	V
DVDD28_MSDC1	Digital power input for MSDC1 IO	1.7	3.6	V
DVDD28_MSDC2	Digital power input for MSDC2 IO	1.7	3.6	V
DVDD12_EMI	Digital power input for EMI	1.14	1.3	V
VCCK	Digital power input for core	0.765	1.265	V
VCCK_VPROC	Digital power input for GPU	0.765	1.265	V

Warning: Stressing the device beyond the absolute maximum ratings may cause permanent damage. These are stress ratings only.

2.2.2 Recommended Operating Conditions

Table 2-6. Recommended operating conditions for power supply

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
DVDD18_PLLGP	Analog power input 1.8V for PLL	1.7	1.8	1.89	V
AVDD18_AP	Analog power input 1.8V for AuxADC, TSENSE	1.71	1.8	1.89	V
AVDD18_MD	Analog power input 1.8V for BBTX, BBRX	1.71	1.8	1.89	V
AVDD28_DAC	Analog power input 2.8V for APC	2.66	2.8	2.94	V
DVDD18_MIPITX	Analog power for MIPI DSI	1.71	1.8	1.89	V
DVDD18_MIPIIO	Analog power for MIPI CSI	1.71	1.8	1.89	V
AVDD33_USB	Analog power 3.3V for USB	3.135	3.3	3.465	V
AVDD18_USB	Analog power 1.8V for USB	1.71	1.8	1.89	V
AVDD18_MEMPLL	Analog power for MEMPLL	1.71	1.8	1.89	V
DVDD18_MSDC0	Digital power input for MSDC0 IO	1.7	1.8	1.95	V
DVDD18_IO0	Digital power input for IO	1.7	1.8	1.9	V
DVDD18_IO1	Digital power input for IO	1.7	1.8	1.9	V
DVDD18_IO2	Digital power input for IO	1.7	1.8	1.9	V
DVDD18_IO3	Digital power input for IO	1.7	1.8	1.9	V
DVDD18_IO4	Digital power input for IO	1.7	1.8	1.9	V
DVDD18_EFUSE	Digital power input for efuse IO	1.8	1.9	2.0	V

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Symbol or pin name	Description	Min.	Typ.	Max.	Unit
DVDD28_BPI	Digital power input for BPI	1.7	1.8	1.9	V
		2.7	3.3	3.6	
DVDD28_MSDC1	Digital power input for MSDC1 IO	1.7	1.8	1.95	V
		2.7	3.3	3.6	
DVDD28_MSDC2	Digital power input for MSDC2 IO	1.7	1.8	1.95	V
		2.7	3.3	3.6	
DVDD12_EMI	Digital power input for EMI (LPDDR2)	1.14	1.2	1.3	V
	Digital power input for EMI (LPDDR3)	1.14	1.2	1.3	
VCCK	Digital power input for core	1.09	1.15	1.265	V
VCCK_VPROC	Digital power input for processor	1.09	1.15	1.265	V

2.2.3 Storage Condition

1. Shelf life in sealed bag: 12 months at < 40°C and < 90% relative humidity (RH).
2. After bag opened, devices subjected to infrared reflow, vapor-phase reflow, or equivalent processing must be:
   - Mounted within 168 hours at factory conditions of 30°C/60% RH, or
   - Stored at 20% RH.
3. Devices require baking before mounting, if:
   - 192 hours at 40°C +5°C/-0°C and < 5% RH for low temperature device containers, or
   - 24 hours at 125°C +5°C/-0°C for high temperature device containers.

2.2.4 AC Electrical Characteristics and Timing Diagram

2.2.4.1 External Memory Interface for LPDDR2

The external memory interface, shown in Figure 2-2, Figure 2-3 and Figure 2-4, is used to connect LPDDR2 device for MT6592. It includes pins ED_CLK, ED_CLK_B, ECKE, ECS#, EBA[2:0], EDQS[3:0], EDQS#[3:0], EA[9:0] and ED[31:0]. Table 2-5 summarizes the symbol definition and the related timing specifications.

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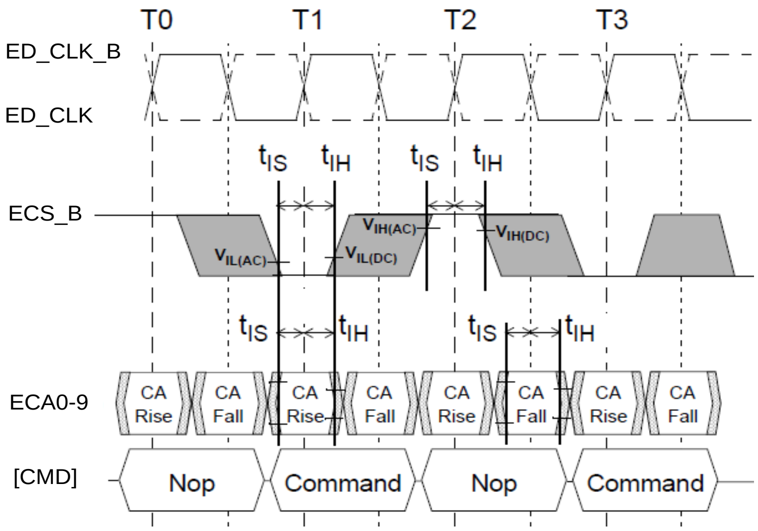

Figure 2-3. Basic timing parameter for LPDDR2 commands

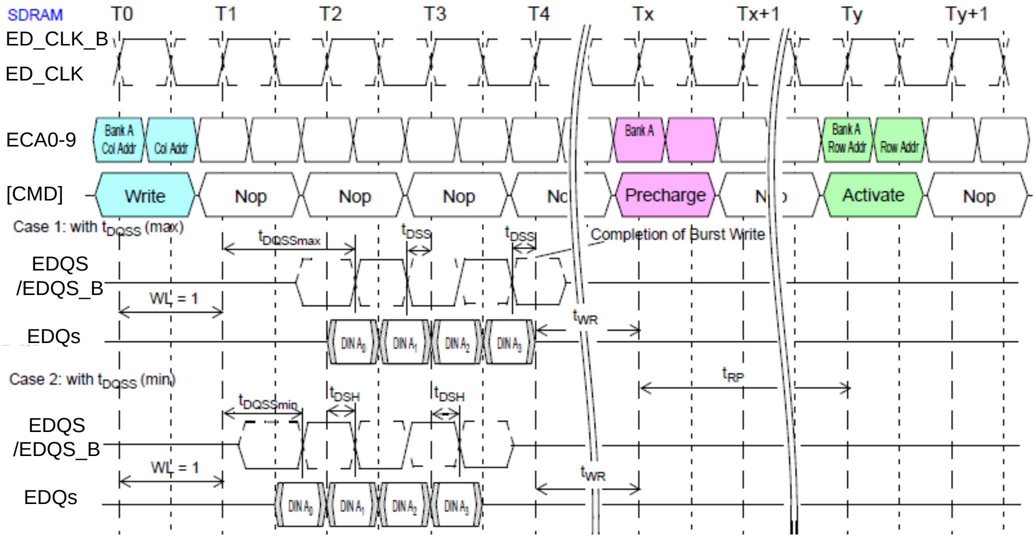

Figure 2-4. Basic timing parameter for LPDDR2 write

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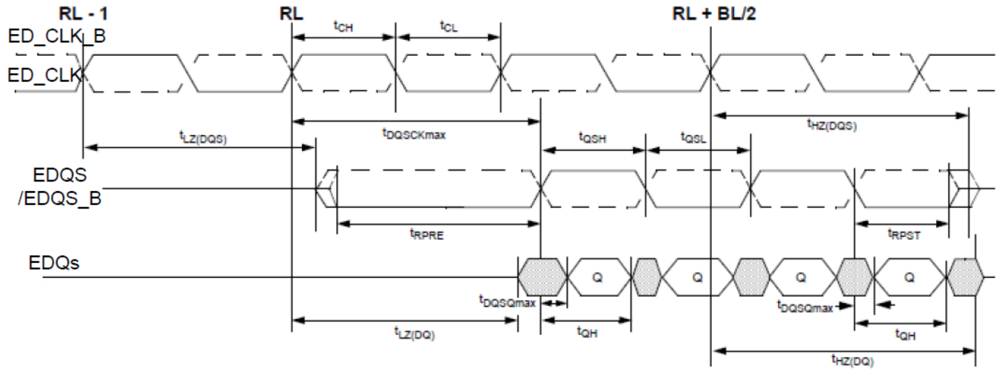
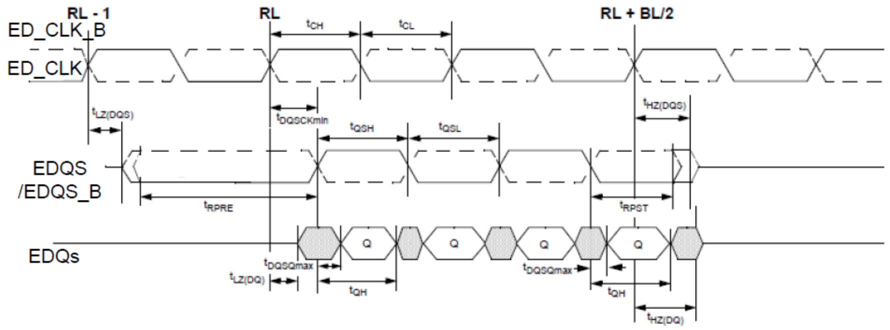


Data output (read) timing ($t_{DQSCKmax}$)



Data output (read) timing ($t_{DQSCKmin}$)

Figure 2-5. Basic timing parameter for LPDDR2 read

Table 2-7. LPDDR2 AC timing parameter table of external memory interfaces

Symbol	Description	Min.	Typ.	Max.	Unit
tCK	Clock cycle time	3.75		8	ns
tDQSCK	DQS output access time from CK/CK’	2.5		5.5	ns
tCH	Clock high level width	0.45		0.55	tCK
tCL	Clock low level width	0.45		0.55	tCK
tHP	Clock half period	0.45		0.55	tCK
tDS	DQ & DM input setup time	0.43			ns
tDH	DQ & DM input hold time	0.43			ns
tDQSS	Write command to 1st DQS latching transition	0.75		1.25	tCK
tDSS	DQS falling edge to CK setup time	0.2			tCK
tDSH	DQS falling edge hold time from CK	0.2			tCK
tIS	Address & control input setup time	0.46			ns
tIH	Address & control input hold time	0.46			ns
tLZ(DQS)	DQS low-impedance time from CK/CK’	tDQSCK (Min.) – 300			ns
tHZ(DQS)	DQS high-impedance time from CK/CK’	tDQSCK (Max.) – 100			ns
tLZ(DQ)	DQ low-impedance time from CK/CK’	tDQSCK (Min.) – (1.4×tQHS (Max.))			ns

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Symbol	Description	Min.	Typ.	Max.	Unit
tHZ(DQ)	DQ high-impedance time from CK/CK’	tDQSCK (Max.) + (1.4×tDQSQ (Max.))			ns
tDQSQ	DQS-DQ skew	0.34			ns
tQHP	Data half period	Min. (tQSH, tQSL)			tCK
tQHS	Data hold skew factor	0.4			ns
tQH	DQ/DQS output hold time from DQS	tQHP – tQHS			ns
tDQSH	DQS input high-level width	0.4			tCK
tDQSL	DQS input low-level width	0.4			tCK
tQSH	DQS output high pulse width	tCH – 0.05			tCK
tQSL	DQS output low pulse width	tCL – 0.05			tCK
tMRW	MODE register Write command period	5			tCK
tMRR	MODE register Read command period	2			tCK
tRPRE	Read preamble	0.9		1.1	tCK
tRPST	Read postamble	tCL – 0.05			tCK
tRAS	ACTIVE to PRECHARGE command period	3			tCK
tRC	ACTIVE to ACTIVE command period	6			tCK
tRFC	AUTO REFRESH to ACTIVE/AUTO REFRESH command period	56			tCK
tRCD	ACTIVE to READ or WRITE delay	3			tCK
tRP	PRECHARGE command period	3			tCK
tRRD	ACTIVE bank A to ACTIVE bank B delay	2			tCK
tWR	WRITE recovery time	3			tCK
tWTR	Internal write to READ command time	2			tCK
tXSR	SELF REFRESH exit to the next valid command	40			tCK
tXP	EXIT power-down to the next valid command delay	2			tCK
tCKE	CKE min. pulse width (high & low pulse width)	2			tCK

2.3 System Configuration

2.3.1 Constant Tie Pins

Table 2-8. Constant tied pins of MT6592

Pin name	Description
TESTMODE	Test mode (tie to GND)
FSOURCE_P	EFUSE blowing (tie to GND)

2.4 Power-on Sequence

The power-on/off sequence with XTAL is shown in the following figure:

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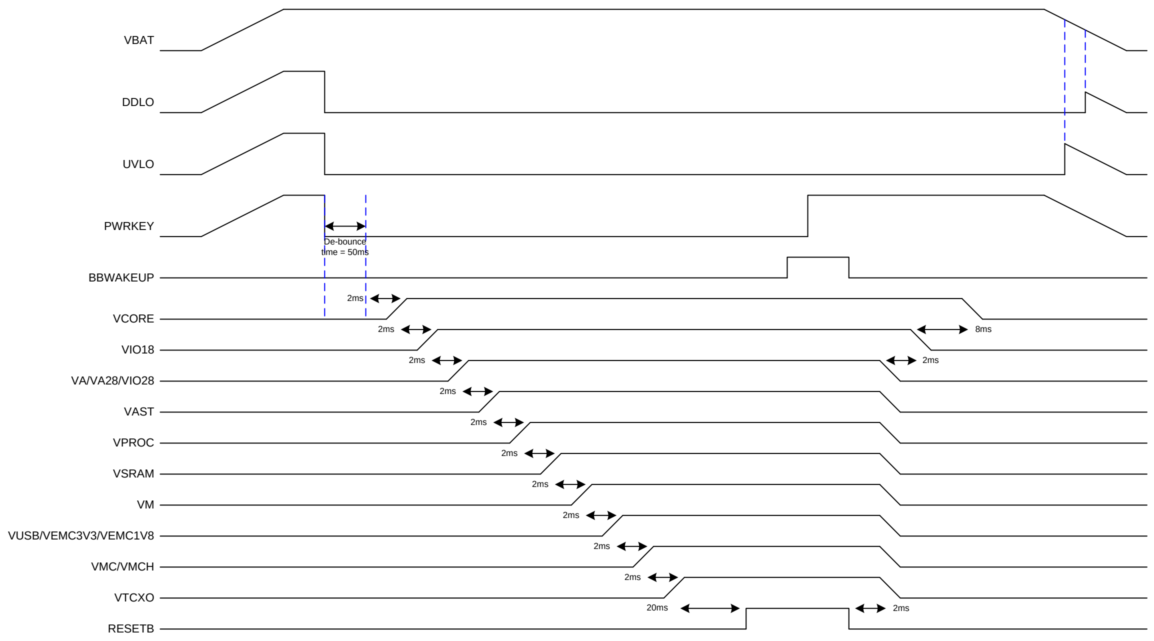

Figure 2-6. Power on/off sequence with and without XTAL

Note that the above figure shows one power-on/off condition with and without XTAL. The external PMIC MT6322 for application processor MT6592 handles the power ON and OFF of the handset. The following three different methods switch on the handset (when VBAT ≥ 3.2V):

1. Pulling PWRKEY low (The user presses PWRKEY.)
2. Pulling BBWAKEUP high
3. Valid charger plug-in

Pulling PWRKEY low is a normal way to turn on the handset, which turns on regulators as long as the PWRKEY is kept low. MT6322 outputs reset signal RESETB to MT6592 SYSRSTB input. After SYSRSTB is de-asserted, the microprocessor starts and pulls BBWAKEUP high. After that PWRKEY can be released, pulling BBWAKEUP high will also turn on the handset. This is the case when the alarm in the RTC expires.

Besides, applying a valid external supply on CHRIN will also turn on the handset. However, if the battery is in the UV state (VBAT < 3.2V), the handset cannot be turned on in any way.

The UVLO function in MT6322 prevents system startup when initial voltage of the main battery is below the 3.2V threshold. When the battery voltage is bigger than 3.2V, the UVLO comparator switches and threshold are reduced to 2.75V, which allows the handset to start smoothly unless the battery decays to 2.75V and below.

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Once MT6322 enters the UVLO state, it draws very low quiescent current. The VRTC LDO will still be active until the DDLO disables it.

The timing diagram also shows the power-on/off sequence without XTAL. VTCXO is always turned on when VBAT is above the DDLO threshold.

2.5 Analog Baseband

2.5.1 Introduction

To communicate with analog blocks, a common control interface for all analog blocks is implemented. In addition, there are some dedicated interfaces for data transfer. The common control interface translates the APB bus write and read cycle for specific addresses related to analog front-end control. During the writing or reading of any of these control registers, there is a latency associated with the transfer of data to or from the analog front-end. Dedicated data interface of each analog block is implemented in the corresponding digital block. An analog block includes the following analog functions for the complete GSM/GPRS/WCDMA base-band signal processing:

Base-band Rx: For I/Q channels base-band A/D conversion
Base-band Tx: For I/Q channels base-band D/A conversion and smoothing filtering
RF control: One DAC for automatic power control (APC) is included.The output is provided to external RF power amplifier respectively. One more DAC for voltage bias control (VBIAS) is included for WCDMA system, and the output is provided to the external RF power amplifier.
Auxiliary ADC: Provides an ADC for the battery and other auxiliary analog functions monitoring.

- Clock generation: One clock-squarer for shaping the input sinwave clock and 10 PLLs providing clock signals to base-band TRx, DSP, MCU, USB, MSDC units.

2.5.2 Features

The analog blocks include the following analog functions for complete GSM/GPRS/WCDMA base-band signal processing:

- BBRX
- BBTX
- APC-DAC
- VBIAS-DAC
- AUXADC
- Phase locked loop
- Temperature sensor

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2.5.3 Block Diagram

2.5.3.1 BBRX

2.5.3.1.1 Block Descriptions

The receiver (Rx) performs baseband I/Q channels downlink analog-to-digital conversion:

1. Analog input multiplexer: For each channel, a 2-input multiplexer is included.
2. A/D converter: 2 high performance sigma-delta ADCs perform I/Q digitization for further digital signal processing.

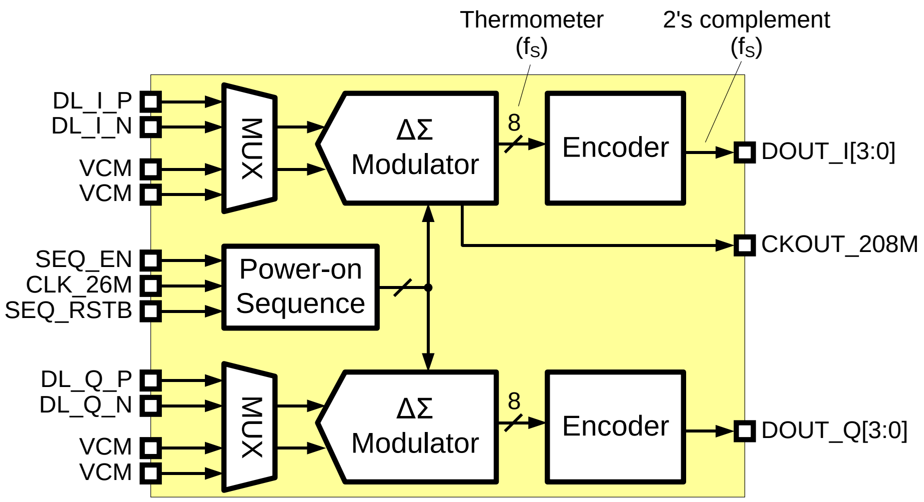

Figure 2-7. Block diagram of BBRX-ADC

2.5.3.1.2 Functional Specifications

See the table below for the functional specifications of the base-band downlink receiver.

Table 2-9. Baseband downlink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Differential analog input voltage (peak-to-peak)			2.4	V
ICM	Common mode input current magnitude			1	uA
VCM	Common mode input voltage	0.65	0.7	0.75	V
FC	Input clock frequency		208		MHz
	Input clock duty cycle	49.5	50	50.5	%
	Input clock period jitter, DC mode			0.14	% (rms)
	Input clock period jitter, SC mode & GSM mode			0.61	% (rms)

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Symbol	Parameter	Min.	Typ.	Max.	Unit
RIN	Differential input resistance	11.2	16	20.8	kΩ
FS	Output sampling rate		208		MSPS
VOS	Differential input referred offset			10	mV
SIN	Signal to in-band noise – SC mode, 2.4Vpp (2.7MHz) sinewave, 1kHz ~ 2.1MHz band – TD-SCDMA mode, 2.4Vpp (1.6MHz) sinewave, 1kHz ~ 625kHz band – GSM mode: 2.4Vpp(570kHz) sinewave, 70kHz ~ 270kHz band	72 77 84	75 80 87		dB dB dB
DVDD18	Digital power supply	1.7	1.8	1.9	V
AVDD18	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	−20		80	°C
	Current consumption (per channel) – Power-up – Power-down			3 1	mA uA

2.5.3.2 BBTX

2.5.3.2.1 Block Descriptions

BBTX includes two channels of DACs with the first order low pass filter. The DACs are PMOS current-steering topology with NMOS constant sinking current, and the active RC filter performs current to the voltage buffer.

The bitwidth of DACs is 10-bit which is encoded into 7 bits of thermometer code and 7 binary code by mixedsys hardware. The encoded bits are timing synchronized by D-type flip-flop which is toggled by the analog local clock. MD-PLL deliver 832MHz differential clock to BBTX. A clock divider translates 832MHz to 416MHz for DACs and AFIFO inside the mixedsys.

The IO power, DVDD18_MD, is regulated to a voltage around 1.55V to supply analog component, and the required bias currents are generated by BBRX.

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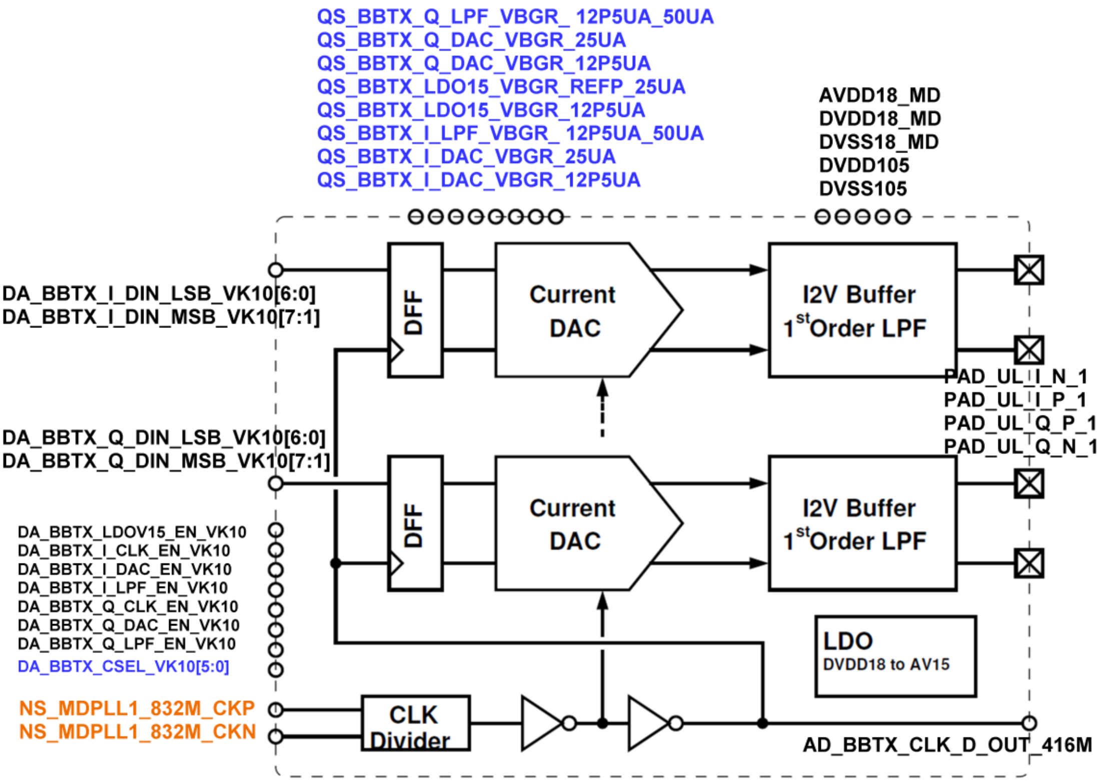

Figure 2-8. Block diagram of BBTX-DAC

2.5.3.2.2 Functional Specifications

Table 2-10. Baseband uplink transmitter specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit.
V_{ocm}	DC output common mode voltage	0.615	0.65	0.685	V
I_K	HF Leakage current @ supply, Irms @416*2=832MHz			3.5	uA
V_{fs}	DAC output swing		2100		mV
N	DAC resolution		10.0		bit
F_s	Sampling clock		416		MHz
I_{mis}	1-sgma DAC unit cell mismatch			1	%
G_{mis}	3-sigma I/Q gain mismatch	-0.2		0.2	dB
V_{os_T}	3-sigma output differential DC offset over temp.			4	mV
V_{os}	3-sigma output differential DC offset			10	mV
F_{3dB}	3dB corner freq.	20	25	30	MHz
S_{LPF}	LPF selectivity @832MHz	28			dB

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Symbol	Parameter	Min.	Typ.	Max.	Unit.
N_{OOB}	Output noise level @45MHz		15.1	30.1.	nVrms/sqrt(Hz)
CN	Signal to noise ratio@45MHz		-146	-140	dBc/Hz
IM3	In-band two-tone test swing V1=V2=290/sqrt(2) mV		-60	-56	dBc
T	Operating temperature	-20		80	°C
	Current consumption Power-up Power-down		5.3 10		mA uA

2.5.3.3 APC-DAC

2.5.3.3.1 Block Descriptions

See the figure below. APC-DAC is designed to produce a single-ended output signal at APC pin.

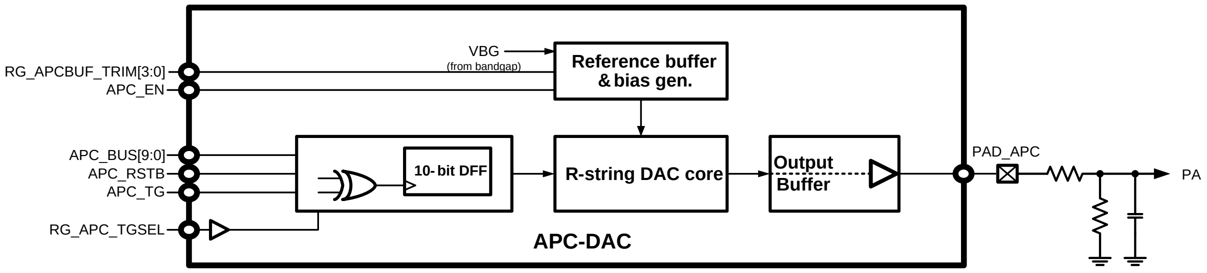

Figure 2-9. Block diagram of APC-DAC

2.5.3.3.2 Functional Specifications

See the table below for the functional specifications of the APC-DAC.

Table 2-11. APC-DAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
F_S	Clock rate	1.0833		2.1666	MS/s
SNDR	Signal-to-noise-and-distortion ratio (10kHz sine wave with 1.0V swing)		50		dB
T_S	Settling time (99% full-swing settling)			5	us
$V_{O,max}$	Maximum output			AVDD – 0.2	V

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Symbol	Parameter	Min.	Typ.	Max.	Unit
C_L	Output loading capacitance		220	2200	pF
DNL	Differential nonlinearity (code 30 ~ 970)		±1.0		LSB
INL	Integral nonlinearity (code 30 ~ 970)		±2.0		LSB
DVDD	Digital power supply	0.9	1.0	1.1	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	–20		85	°C
I_{ON}	Current consumption (power-on state)		350		uA
I_{OFF}	Current consumption (power-down state)			20	uA

2.5.3.4 VBIAS-DAC

2.5.3.4.1 Block Descriptions

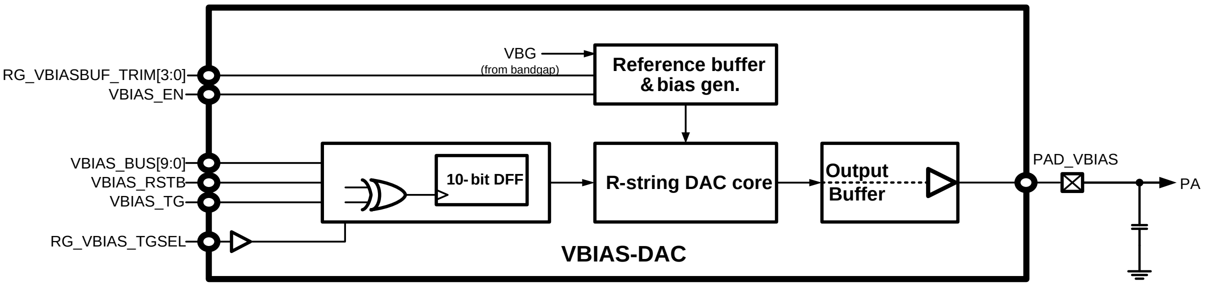

Figure 2-10. Block diagram of VBIAS-DAC

2.5.3.4.2 Functional Specifications

See the table below for the functional specifications of VBIAS-DAC.

Table 2-12. VBIAS-DAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
F_S	Clock rate	1.0833		2.1666	MS/s
SNDR	Signal-to-noise-and-distortion ratio (10kHz sine wave with 1.0V swing)		50		dB
T_S	Settling time (99% full-swing settling)			5	us
$V_{O,max}$	Maximum output			AVDD – 0.2	V
C_L	Output loading capacitance		1000		pF

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Symbol	Parameter	Min.	Typ.	Max.	Unit
DNL	Differential nonlinearity (code 20 ~ 970)		±1.0		LSB
INL	Integral nonlinearity (code 20 ~ 970)		±2.0		LSB
DVDD	Digital power supply	0.9	1.0	1.1	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	–20		85	°C
I_{ON}	Current consumption (power-on state)		350		uA
I_{OFF}	Current consumption (power-down state)			20	uA

2.5.3.5 AUXADC

2.5.3.5.1 Block Descriptions

The auxiliary ADC includes the following functional blocks:

1. Analog multiplexer: Selects signal from one of the auxiliary input channels. There are 16 input channels of AUXADC. Some are for internal voltage measuring and some for external voltage measuring. Environmental messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
2. 12-bit A/D converter: Converts the multiplexed input signal to 12-bit digital data.

See
Table ***2-13. Definitions of AUXADC channels*** for brief descriptions of AUXADC input channels.

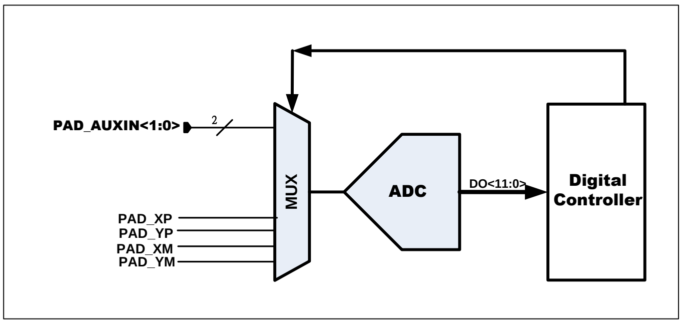

Figure 2-11. Block diagram of AUXADC

Table 2-13. Definitions of AUXADC channels

AUXADC channel ID	Description
Channel 0	External use (AUX_IN0)

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AUXADC channel ID	Description
Channel 1	External use (AUX_IN1)
Channel 2	NA
Channel 3	NA
Channel 4	NA
Channel 5	NA
Channel 6	NA
Channel 7	NA
Channel 8	NA
Channel 9	NA
Channel 10	NA
Channel 11	NA
Channel 12	XM
Channel 13	XP
Channel 14	YP
Channel 15	YM

2.5.3.5.2 Functional Specifications

See the table below for the functional specifications of auxiliary ADC.

Table 2-14. AUXADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		12		Bit
FC	Clock rate		4		MHz
FS	Sampling rate @ N-Bit		4/(N+4)		MSPS
	Input swing	0.05		1.45	V
CIN	Input capacitance Unselected channel Selected channel		50 4		fF pF
RIN	Input resistance Unselected channel	400			MΩ
	Clock latency		N+4		1/FC
DNL	Differential nonlinearity		+1.0/-1.0		LSB
INL	Integral nonlinearity		+2.0/-2.0		LSB
SINAD	Signal to noise and distortion ratio (1kHz full swing input & 1.0833MHz clock rate)	62	68		dB

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Symbol	Parameter	Min.	Typ.	Max.	Unit
DVDD	Digital power supply	1.0	1.1	1.2	V
AVDD	Analog power supply	1.75	1.8	1.85	V
T	Operating temperature	-20		80	°C
	Current consumption Power-up Power-down		400 1		uA uA

2.5.3.6 Clock Squarer

2.5.3.6.1 Block Descriptions

For most VCXO, the output clock waveform is sinusoidal with too small amplitude (about several hundred mV) to make digital circuits function well. The clock squarer is designed to convert such a small signal to a rail-to-rail clock signal with excellent duty-cycle.

2.5.3.6.2 Functional Specifications

See the table below for the functional specifications of clock squarer.

Table 2-15. Clock squarer specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency	13	26		MHz
Fout	Output clock frequency	13	26		MHz
Vin	Input signal amplitude	350	500	1,000	mVpp
DcycIN	Input signal duty cycle		50		%
DcycOUT	Output signal duty cycle	DcycIN-5		DcycIN+5	%
TR	Rise time on pin CLKSQOUT			5	ns/pF
TF	Fall time on pin CLKSQOUT			5	ns/pF
DVDD	Digital power supply	1.0	1.1	1.2	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		500		uA

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2.5.3.7 Phase Locked Loop

2.5.3.7.1 Block Descriptions

There are total 11 PLLs in PLL macro, providing several clocks for CPU, BUS, modem, analog modem, MSDC and image-sensor.

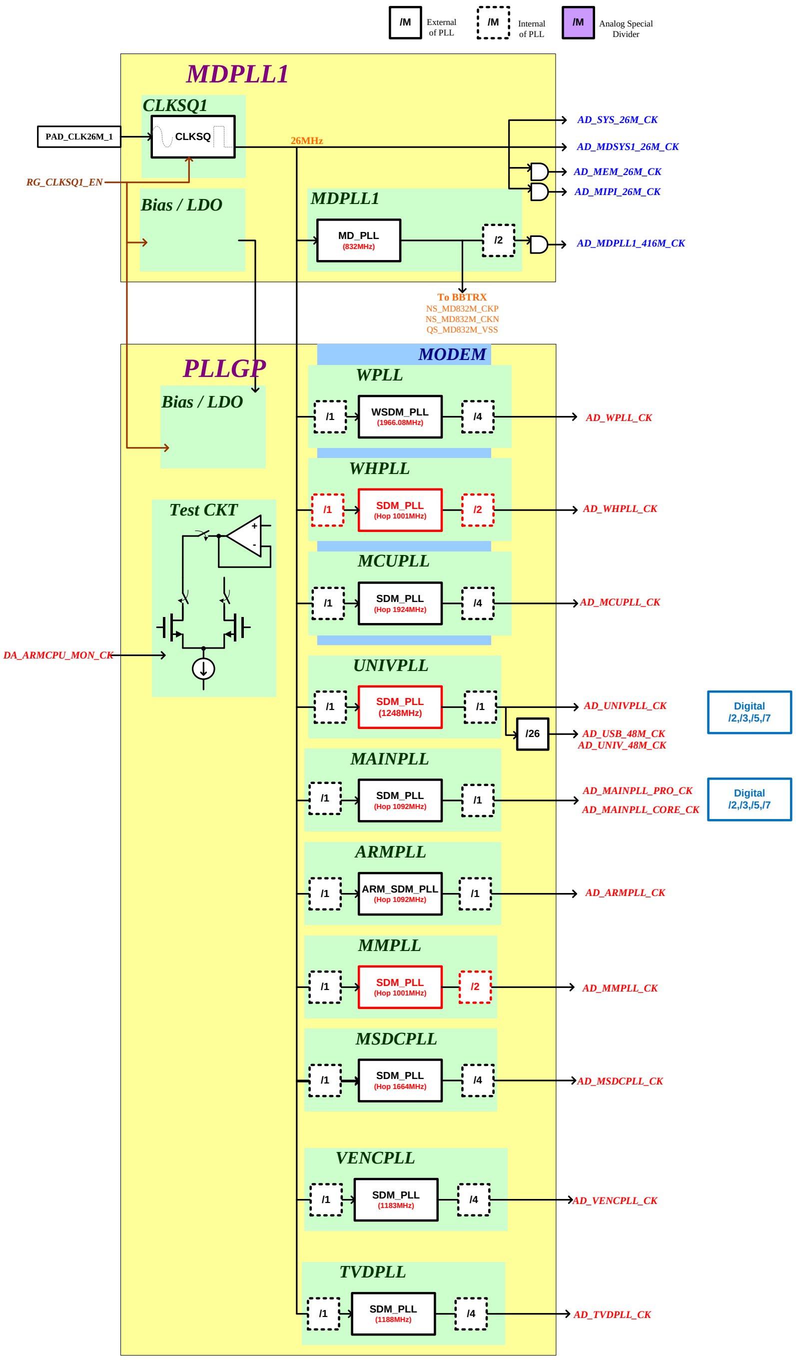

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Figure 2-12. Block diagram of PLL

2.5.3.7.2 Functional Specifications

See the table below for the functional specifications of PLL.

Table 2-16. ARMPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		1092		MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		30		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1.2		mA
	Power-down current consumption			0.1	uA

Table 2-17. MAINPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		1092		MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1.2		mA
	Power-down current consumption			0.1	uA

Table 2-18. MMPLL specifications

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Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		500.5		MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 2-19. UNIVPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	1248	N/A	MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 2-20. MSDCPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		416		MHz
	Settling time		20		us

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 2-21. MDPLL1 specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	416	N/A	MHz
	Settling time		100		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		30		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		2.5		mA
	Power-down current consumption			0.1	uA

Table 2-22. WPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	491.52	N/A	MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V

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Symbol	Parameter	Min.	Typ.	Max.	Unit
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 2-23. WHPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		500.5		MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 2-24. MCUPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		481		MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

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Table 2-25. VENCPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		295.75		MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 2-26. TVDPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		148.5		MHz
	Settling time		20		Us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

2.5.3.8 Temperature Sensor

2.5.3.8.1 Block Descriptions

In order to monitor the temperature of CPUs, several temperature sensors are provided. The temperature sensor is made of substrate BJT in the CMOS process. The voltage output of temperature sensor is measured by AUXADC.

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2.5.3.8.2 Functional Specifications

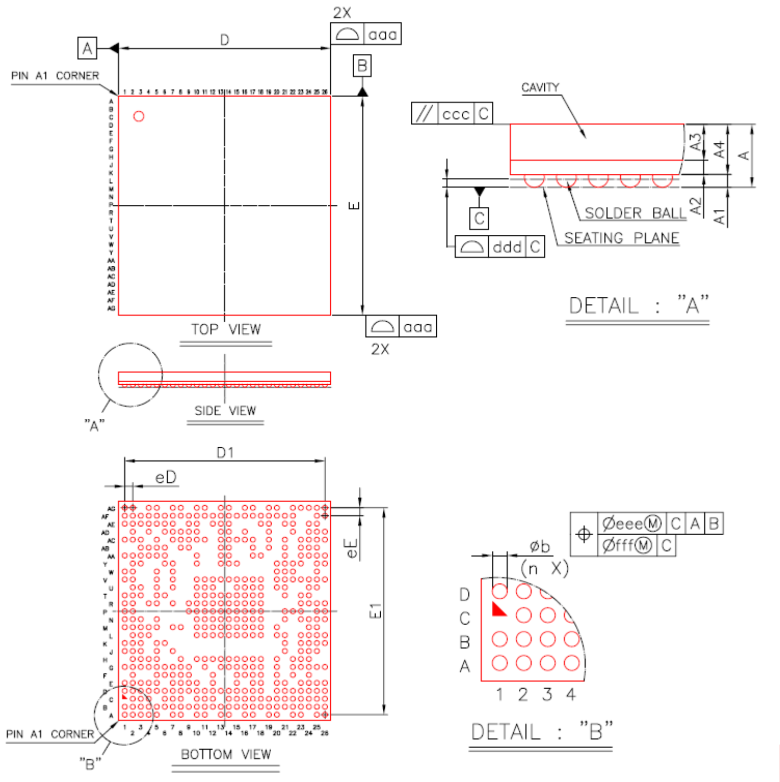
See the table below for the functional specifications of temperature sensor.

Table 2-27. Temperature sensor specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Resolution		0.15		°C
	Temperature range	0		85	°C
	Accuracy	-5		5	°C
	Active current		300		uA
	Quiescent current		3		uA

2.6 Package Information

2.6.1 Package Outlines



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type			VFMIP		
Body Size	X	D	10.50	10.60	10.70
	Y	E	10.90	11.00	11.10
Ball Pitch	X	eD	0.40		
	Y	eE	0.40		
Total Thickness		A	–	–	0.90
Mold Thickness		A3	0.45 Ref.		
Substrate Thickness		A2	0.15 Ref.		
Substrate+Mold Thickness		A4	0.55	0.60	0.65
Ball Diameter			0.25		
Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa	0.05		
Mold Flatness		ccc	0.10		
Coplanarity		ddd	0.08		
Ball Offset (Package)		eee	0.15		
Ball Offset (Ball)		fff	0.05		
Ball Count		n	475		
Edge Ball Center to Center	X	D1	10.00		
	Y	E1	10.40		

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*Figure 2-13. Outlines and dimensions of FCCSP 10.6mm*11.0mm, 475-ball, 0.4mm pitch package*

2.6.2 Thermal Operating Specifications

Table 2-28. Thermal operating specifications

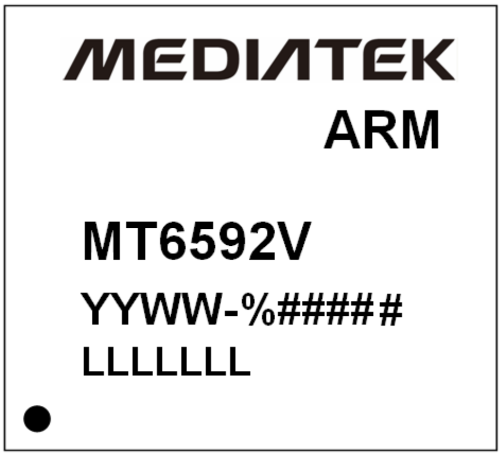
Symbol	Description	Value	Unit	Notes
	Maximum operating junction temperature	125	°C	
	Package thermal resistances in nature convection	25.8	°C/Watt	

2.6.3 Lead-free Packaging

MT6592 is provided in a lead-free package and meets RoHS requirements.

2.7 Ordering Information

2.7.1 Top Marking Definition



- YYWW: Date Code
- %: Functional Code
  W: W-CDMA
  T: TD-SCDMA
  E: EDGE
- #####: Subcontractor Code
- LLLLLLL: Lot Number

Figure 2-14. Top mark of MT6592

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